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Auxiliary Roles in STT-MRAM Memory

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Auxiliary Roles in STT-MRAM Memory

by

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A dissertation submitted in partial fulfillment
of the requirements for the degree of
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DEDICATION

To my parents and sister.

ACKNOWLEDGMENTS

A journey of close to four years is nearing its end. I would acknowledge it has been one of the most fulfilling years of my life where failures met successes, rejects met accepts and learning met obstacles. Along its way I have met various individuals who have uniquely contributed with their meticulous hands to shape it the way it is today. The first person is my advisor Dr. Sanjukta Bhanja. Our first telephonic conversation goes back to winter of 2009 when I had requested information for a graduate student position. I got a fresh opportunity to restart my career and fulfill my dreams. Her increased belief in me increased my confidence. She went on to nominate me for the Presidential Doctoral Fellowship, the highest fellowship awarded by the university. Here I would also like to thank Dr. Morgera for the nomination. In these years Dr. Bhanja gave me the freedom to explore, gave me the scope to imagine endlessly and appreciated all my creative efforts. With time she continued to assign me with greater responsibilities to grow in the role of a technical leader and engaging me in activities beyond research. She encouraged me to attend conferences and involve in outreach. Her patience has been remarkable when I failed and her feedback has been critical to my improvement. I would say that she has been one of my best critics in these years. Ending without acknowledging some of our open discussions and arguments in topics beyond research will only result in not acknowledging one vital skill that I acquired, the skill to persuasively and fearlessly defend my thoughts as a Ph.D. student.

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Dr. Mumcu has been the professor known in our department to challenge his students. My first association with him was in his RF class of Fall 2011. The class was both thrilling and fun-filled, wrapped with challenges and stricter deadlines at the end of every week. The ardent desire to beat those challenges and kept alive by his constant encouragement has on multiple accounts brought the best out of me, the surprising potentials within me. This desire was further fueled by his positive criticisms, his belief in me, his offering of tougher challenges, his embedding within me a never give up attitude and his devoting selfless hours to debugging our homework problems whenever we showed up at his door. Needless to mention I went on to take all of his courses in the next two years ending each of them with greater and greater self-confidence. Dr. Mumcu has been one of my pillars of inspiration.

It was in the Spring of 2011 that I enrolled in Dr. Sarkar's class of probability estimation modeling and inference. The learning curve in class was steep, almost vertical and the experience everlasting. The assignments were equally challenging. I remember him as the awe-inspiring professor who did all the mind-blowing intricate derivations by hand in class and had all the admirations I could have for a professor at that time. He has since then been one of my role models for dedication, precision and integrity. I thank him for the example he set to us and his support on numerous occasions later in my life.

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABSTRACT

Computer memories now play a key role in our everyday life given the increase in the number of connected smart devices and wearables. Recently post-CMOS memory technologies are gaining significant research attention along with the regular ones. Spin Transfer Torque Magnetoresistive RAM (STT-MRAM) is one such post-CMOS memory technology with a rapidly growing commercial interest and potential across diverse application platforms. Research has shown the ability of STT-MRAM to replace different levels of memory hierarchy as well. In brief, STT-MRAM possesses all the favorable properties of a universal memory technology. In this dissertation we have explored the roles of this emerging memory technology beyond traditional storage. The purpose is to enhance the overall performance of the application platform that STT-MRAM is a part of. The roles that we explored are computation and security. We have discussed how the intrinsic properties of STT-MRAM can be used for computation and authentication. The two properties that we are interested in are the dipolar coupling between the magnetic memory cells and the variations in the geometries of the memory cell. Our contributions here are a 22nm CMOS integrated STT-MRAM based logic-in-memory architecture and a geometric variation based STT-MRAM signature generation. In addition we have explored the device physics and the dynamics of STT-MRAM cells to propose a STT based clocking mechanism that is friendlier with the logic-in-memory setup. By investigating the logic layouts and propagation style in the architecture, we have also proposed different techniques that can improve the logic density and performance of the architecture.

CHAPTER 1

INTRODUCTION

1.1 Background

Memory is key to human consciousness and the linchpin of our identity [1]. Thomas Reid says "The evidence we have of our identity, as far back as we remember is grounded on memory." Memory has also continued to baffle our minds for centuries so much so that various attempts have been made to analyze it. Societies have also rested on its potentials for centuries to transmit texts with inordinate fidelity like the Vedas in Indian Literature. Some of the early references from Egypt and Greece (4000-1000BC) describes the governance of memory with gods and goddesses [2]. While the first documents of memory scholarship dates back to Dialexeis (5th century BC), it was not until Plato and Aristotle that memory was studied more theoretically. Plato used different metaphors like wax tablets and an aviary to describe the mechanisms of remembering and recalling. A few centuries later St. Augustine (354-430AD) compared memory to a cave with numerous mysterious recesses that are used to receive, store and retrieve information. He wonderfully proclaims "Great is the power of memory,...a large and boundless inner hall!" [2]. Philosophers have also not failed to recognize the fragility of this mystic human faculty. In the first century Pliny describes the susceptibility of memory to apprehensions, diseases and accidents. In the Renaissance period, the interest shifted more towards visual aids as Francis Bacon describes writing to be a great aid to memory. Among the other patrons of memory include poets and writers from different ages like Samuel Rogers, Emily Dickinson and Tony Morrison. The trend among modern psychologists is to use more contemporary examples like vibrating

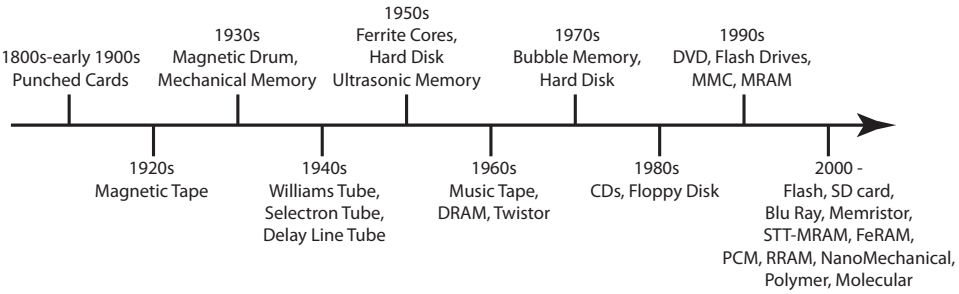


Figure 1.1: Popular computer memories in different decades.

particles, weathered signposts, electrical condensers and holograms to model memory. Very interestingly one of the recent models is after memory's greatest aid, the computer memory.

In computers the memory is that inner hall, which is used to store data and instructions. It is also a major decision maker to a computer's performance so much so that it has for decades driven scientists continually in the pursuit of various materials and technologies. With this continual effort the computer memory has not only grown in density over time, it has also significantly improved in speed. The punch cards that were popular in the early part of the twentieth century required hundreds of milliseconds to process a single card of less than 1Kb capacity [3, 4] while today's flash memories coming in finger-sizes can achieve a speed of 5 Gbps. Fig. 1.1 compiles a history of the development in computer memories [5, 6].

Today different memory technologies are investigated to meet different application demands. The worth of a memory technology is usually estimated with the help of certain key properties like cell size, access time, access mode, endurance, retention, power/energy, cost per bit, non-volatility and scalability. Here we will first discuss the property definitions before comparing some of the emerging memory technologies. The cell size defines the bit area in units of minimum feature size (F). Smaller the cell size, the denser is the memory. The access time refers to the read/write latency and the access mode refers to the random or block access of memory. Both impact the memory bandwidth. The endurance is the memory's ability to withstand the number of write, program, erase and read cycles. Retention refers to the length of time that a memory bit can hold onto its state. A memory technology

that can indefinitely hold onto its state without any external help is said to be non-volatile. The write energy for the memory is often the critical factor in the power/energy metrics of a memory technology and the usefulness of the technology. Cost per bit is a function that encompasses different aspects of technology like area, fabrication cost, testing, etc. Finally scalability refers to the scope for high density memories in future technology nodes and is one of the keys to cost reduction per bit. Fig. 1.2 compares different memory technologies on the basis of their above listed memory properties. From the figure it is obvious that the different memory technologies have a tradeoff between properties and the choice of a technology is therefore more application specific. However, in recent times technologies like Spin Transfer Torque Magnetoresistive RAM (STT-MRAM) have shown the potential to replace different levels of memory hierarchy [7] as a projected universal memory technology.

Memory is also fundamental to the vast majority of todays smart devices. It should not take any greater than a mere effort of simply imagining the horrors of losing all the contacts from our cell phones to appreciate the role of memories in our everyday modern life! Samsung the leader in smartphone mentions that consumer expectations of remaining "always-on always-connected" can only be enhanced by the advancement of the memory chip in the device [8]. Samsung is already looking into smart memories that can give high performance, greater energy savings and smaller form factor. Just as it has succeeded with philosophers and psychologists memory has continued to intrigue the minds of engineers and scientists as well. In this dissertation we have joined hands with this group of researchers to stretch the role of a contemporary memory technology beyond that of traditional data storage with the aim to improve the overall computing performance in modern devices.

1.2 Motivation

As the advantages from Dennard scaling are nearing its end, Moore's law is also becoming more questionable in the forthcoming years. Industry and academics have therefore

	Volatile			Non-Volatile				
	SRAM	DRAM		Flash		FeRAM	STT-MRAM	PCM
		Stand-alone	Embedded	NOR Embedded	NAND Stand-alone			
Storage Mechanism	Interlocked logic state	Charge in capacitor		Trapped charge in floating gate or gate insulator		Polarization in ferroelectric cap	Magnetization of ferromagnetic layer	Amorphous and Crystalline phases
Cell Element	6T	1T1C		1T		1T1C	1T1R	1T1R/1D1R
Feature Size, F, nm	45	36	65	90	22	180	65	45
Cell Area F^2	140	6	12-30	10	4	22	20	4
Read Time, ns	0.2	<10	2	15	1e5	40	35	12
Write/Erase Time, ns	0.2	<10	2	1e3/1e7	1e6/1e5	65	35	100
Retention	-	64m	4m	10y	10y	10y	>10y	>10y
Endurance Cycles	>1E16	>1E16	>1E16	1E5	1E4	1E14	>1E12	1E9
Write Operating Voltage V	1	2.5	2.5	10	15	1.3-3.3	1.8	3
Read Operating Voltage V	1	1.8	1.7	1.8	1.8	1.3-3.3	1.8	1.2
Write Energy J/bit	5E-16	4E-15	5E-15	1E-10	2E-16	3E-14	2.5E-12	6E-12

Figure 1.2: Comparison of different memory technologies [9].

got involved in seeking solutions from alternative technologies to meet the ever increasing consumer demands. STT-MRAM, Phase Change Memories (PCM) and Ferroelectric RAM (FeRAM) are some of the competing and promising non-volatile memory technologies listed by ITRS as technologies for future [10] (see Fig. 1.2). But what is so special about STT-MRAM? STT-MRAM is CMOS integrable. When compared to DRAM, STT-MRAM has a higher retention. When compared to SRAM it has a smaller footprint. And when compared to Flash and PCM, STT-MRAM provides unlimited read/write endurance. When compared to FeRAM it has a smaller feature size. In addition, STT-MRAM is also thermally robust and radiation hard [11]. It has also the potential to replace different levels of the memory hierarchy [7]. With its zero leakage property it can also help to develop sustainable platforms for various applications including data centers, which are currently plagued by excess leakage problems [12, 13].

STT-MRAM has already made its way to the market. 64Mb DDR3 compatible STT-MRAM and embedded MRAMs are already commercialized by Everspin Technologies, Inc. [11]. Toshiba has announced its first STT-MRAM based microprocessor cache memory [14]. In

their 2014 Emerging Non-Volatile Memory and Storage Technologies and Manufacturing Report, Coughlin Associates says "MRAM and STT-MRAM will start to replace SRAM and DRAM within the next few years. It is projected that MRAM and STT-MRAM annual shipping capacity will rise from an estimated 80 TB in 2013 to 16.5 PB in 2019 with revenues increasing over the same period from $190 M to $2.1 B." [15]. The thermal robustness and radiation hardness of MRAM has enabled the technology to be implemented from automobiles to outer space. These reports and properties strongly support the universal memory role that researchers have already started assigning to STT-MRAM [16, 17].

Convinced of its potential and universality, our objectives were to investigate this modern memory in unconventional roles beyond that of traditional storage. Our intention was to make the memory self sufficient in small computations and security related operations that can boost the overall performance of a smart device in this connected world. In this dissertation we have focused on using the intrinsic properties of STT-MRAM to design a logic-in-memory architecture and to generate unique digital signatures. While computation within memory can alleviate the Von Neumann bottleneck, a unique digital signature from the memory can combat some of the ever increasing concerns of security and piracy faced by the semiconductor industry. Here we have used the field coupling between closely spaced STT-MRAM cells for computation and the variation in the cell geometry for signature generation and authentication.

1.3 Contribution

When it comes solely to data storage applications, the STT-MRAM cells are placed sufficiently far apart to prevent any interaction between them. By bringing the cells closer we risk interaction but open the scope for computation. In this dissertation we have used this concept to build a computing architecture with STT-MRAM. In memory every cell is integrated to a CMOS access transistor [16]. Reducing their spacing for computing purposes

now generates a pitch constraint from the underlying CMOS metal layer. In this dissertation we have discussed how to resolve this with 22nm CMOS technology and selective integration of access transistors. This logic-in-memory architecture we presented can switch between the logic and memory modes of operation with a clock signal as a classifier. The I/O operations for the architecture include write, clock and read. Here we have described how a CMOS operable low power STT clock can help to selectively clock the cells in the architecture. The clock is used to take the cells to a stationary state on top of the energy barrier that separates the two logical states at room temperature. We have shown that this stationary state can be achieved with the help of STT and a special configuration of the STT-MRAM cells that are already in active use in spin torque oscillators.

Our next I/O contributions include a variability tolerant differential read circuit that uses some of the intrinsic properties of the architecture and the cells. The STT-MRAM cells have different resistances for the 0 and 1 states. In memory their contents are read by comparing them to a reference value that is stored at the midpoint of the 0 and 1 resistances. Instead of reading a cell by comparing it to a reference value, we have proposed reading the output by comparing it to its complement that enhances the sense margin. Cell to cell interaction facilitates the complement generation and eliminates the cost associated with maintaining a precise reference. Further by replicating the output and its complement through coupling and comparing a pair of outputs against a pair of complements we have increased the variability tolerance of the read circuit.

To enable fast simulated verification of the architecture, we have designed Verilog-A macromodels to emulate the memory cells in standalone and computing modes of operation. The models internally run a Finite State Machine that decides the outcome of inter-cell coupling. Verilog-A also can be integrated into Cadence Design Suite and the memory cells can be simulated along with the CMOS access transistors. A common objective of the semiconductor industry is to reduce the logic footprint. Here we have discussed three different

ways in which we can reduce the logic footprint to enhance the overall computing performance of the architecture. The first is by introducing small irregularities in the otherwise regular logic layout. This solves a layout constraint problem, which originates from the inability of dipolar coupling to generate A and ¬A at a distance 'd' from a single variable A. A detailed study of the dipolar coupling based logic computation also reveals a constraint between delay, performance and flexibility of layout. By marginal increment in delay through an additional clock phase we have shown how performance and layout flexibility can be improved. Our next improvement is with the datapath elements. To enhance their performance in the architecture we have come up with a logic partitioning scheme based on Shannon expansion of logic. The algorithm efficiently partitions logic responsibilities between the magnetic and CMOS planes of the architecture. With the new partitioning only the cofactors are computed in the magnetic plane that reduces the footprint and improves the performance.

Finally in this dissertation we have shown how we can extract and digitize the information stored within the intrinsic geometric variations in the memory cells with the help of a simple two step procedure. The information can then be used as digital signatures that are unclonable and are not required to be stored anywhere in the memory. The signatures can help in authentication. The information can also be used for random number generation. We believe these roles supported by intrinsic STT-MRAM properties can boost the overall performance of STT-MRAM and the computing platforms.

1.4 Outline of this Dissertation

The outline of this dissertation is as follows:

(i) Chapter 2 gives a background of STT-MRAM and Nanomagnetic Logic (NML).

(ii) Chapter 3 describes our logic-in-memory architecture, its salient features, its CMOS integration, cell types, logic blocks and logic layout.

(iii) Chapter 4 describes the low power STT clock and CMOS powered write and read from the architecture. A variation tolerant differential read circuit is proposed that leverages from the bit dependency in the architecture.

(iv) Chapter 5 describes a Finite State Machine based Verilog-A macromodel of the logic-in-memory cells that can be integrated to Cadence Design Suite and simulated with CMOS. It then proposes certain low energy extensions of the architecture.

(v) Chapter 6 describes two schemes that can significantly reduce the logic footprint and improve the overall performance of the architecture.

(vi) Chapter 7 describes a logic partitioning scheme between the magnetic and the CMOS planes of the architecture. The scheme is based on Shannon expansion of logic. The improvement in area, energy and delay of critical data path elements are discussed.

(vii) Chapter 8 describes an intrinsic variation based signature generation scheme from STT-MRAM that can be used for autentication.

(viii) Chapter 9 concludes this dissertation.

CHAPTER 2

EMERGING NON-VOLATILE MEMORY AND LOGIC

2.1 Introduction

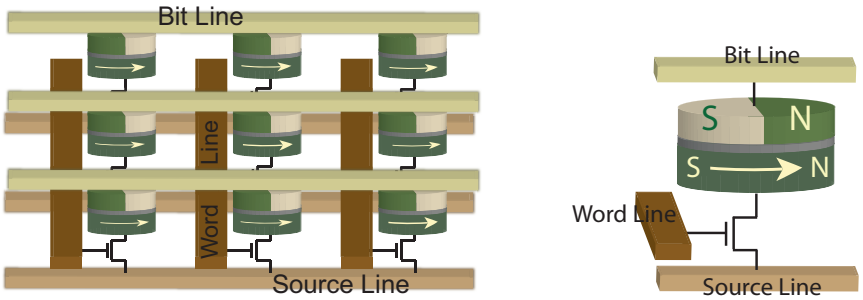
In this chapter we have reviewed the non-volatile STT-MRAM memory, its elemental cells and its key properties. Thereafter we have discussed nanomagnetic logic, a non-volatile logic technology. This chapter should help the readers to gain sufficient understanding of the memory and logic technologies to appreciate their integration in the later chapters of this dissertation.

2.2 STT-MRAM Memory

STT-MRAM is a class of recent non-volatile memories [11, 18, 19, 20, 21, 22]. Combined with the properties of thermal robustness, radiation hardness and unlimited endurance STT-MRAMs have often been projected as universal memories capable of replacing different levels of memory hierarchy [23]. They are already in use as critical storage in industry computing boards, flight control computers and superbike engine controls [11]. In 2012, Everspin Technologies, Inc. has commercialized 64Mb Spin-Torque MRAM [11]. STT-MRAM is also an active research area pursued by several semiconductor giants like Qualcomm Inc., Toshiba Corp., Fujitsu Ltd., Samsung, IBM Corp., Intel Corp. etc.

STT-MRAM has a crossbar memory architecture (see Fig. 2.1a(a)). Each bit is comprised of a magnetic tunnel junction (MTJ) monolithically integrated to an access transistor (see

[0]Parts of this chapter was published in SPIN, World Scientific, 2014, vol. 4(3), " Recent Trends In Spintronics-Based Nanomagnetic Logic", Jayita Das, Syed M Alam, and Sanjukta Bhanja, editor Stuart Parkin. Permission attached in Appendix A.



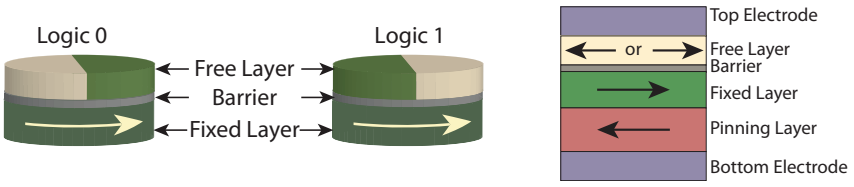
(a) (b)

Figure 2.1: (a) STT-MRAM architecture; (b) 1MTJ/1T STT-MRAM cell.

Fig. 2.1a(b)). Three layers of metal are used for bit-wise access to the memory. Two unique properties of MTJs are used for the two basic memory operations: (i) their response to spin transfer torque (STT) is used for memory write and (ii) their differential electrical resistance is used for memory read. In the following subsections we will focus on MTJs and their unique properties.

2.2.1 Magnetic Tunnel Junction

Magnetic Tunnel Junctions (MTJs) are multi-layered devices. They are composed of a thin insulating layer (barrier) sandwiched between two ferromagnetic (FM) layers (electrodes) [19, 24, 25, 26] (see Fig. 2.2a). The FM layers are single-domain, which means their magnetization is uniform and can be represented by one giant spin [27]. This property is enforced by the dimensions of the layer. The typical dimensions we used in this dissertation are 100×50 nm^2. The MTJs are patterned with a shape anisotropy to generate two stable magnetic states for the FM layer at room temperature. These states are along the easy axis or the longest dimension of the layer. The magnetic polarization of the bottom FM layer is pinned by strong exchange coupling [28] from an adjacent antiferromagnetic layer such as FeMn or IrMn. This layer is called the fixed layer and the layer that pins it is called the pinning layer [21, 29, 30] (see Fig. 2.2b). The magnetization of the top FM layer can be excited with the help of external magnetic fields or with the help of STT [31, 32, 33, 34]



(a) (b)

Figure 2.2: MTJ states and structure. (a) MTJ stable logic configurations (i) Parallel state; (ii) Antiparallel state; (b) MTJ structure and its main constituent layers.

(Section 2.2.4). This is called the free layer. With the help of relative magnetization between the free and the fixed layer, a 1 or 0 is stored in the memory (see Fig. 2.2a).

2.2.2 Tunnel Magnetoresistance

The MTJs also behave like a variable resistor. Their electrical resistance R=G$(\theta)^{-1}$ depends on the relative magnetization angle θ between the free and the fixed layer (Eq. 2.1) [22].

$$G(\theta) = \frac{1}{2}\left(G_P + G_{AP}\right) + \frac{1}{2}\left(G_P - G_{AP}\right) \cdot cos\ \theta \tag{2.1}$$

G_P and G_{AP} are the conductances for $\theta = 0°$ or parallel (logic 0) state (Fig. 2.2a(i)) and $\theta = 180°$ or antiparallel (logic 1) state (Fig. 2.2a (ii)). In MTJs, G_P $(= R_P^{-1})$ > G_{AP} $(= R_{AP}^{-1})$, and their difference Δ G=G_P-G_{AP} is captured by the term Tunnel Magnetoresistance (TMR), defined in Eq. 2.2.

$$TMR = \frac{\Delta G}{G_{AP}} = \frac{R_{AP} - R_P}{R_P} \tag{2.2}$$

This difference in resistance is used to read the memory [19, 22]. High TMR is therefore suited for efficient memory read. Various sensing schemes have been developed where the MTJs are read by comparing against a reference value [35, 36, 37]. The reference is typically maintained at the midpoint of 0 and 1 resistances.

For the curious readers here we will slightly digress to explain the cause of TMR and summarize the milestones in its development. The difference in MTJ resistances for 1 and

0 states arise from the difference in the electronic density of states (DOS) at Fermi level E_F between the spin-up $N_\uparrow(E_F)$ and the spin-down $N_\downarrow(E_F)$ electrons [22]. Since tunneling preserves the electron spin orientation, electron tunneling between the two FM electrodes in MTJs takes place between spin subbands of the same orientation (see Fig. 2.3). The resultant tunneling conductance is therefore proportional to the product of the Fermi level DOS of the two electrodes with the same spin orientation [19, 22]. Since the DOS for the spin subbands is reversed for one of the electrodes between parallel and antiparallel configurations (see Fig. 2.3), the conductances of the two states differ from one another i.e. Δ G$\neq$ 0.

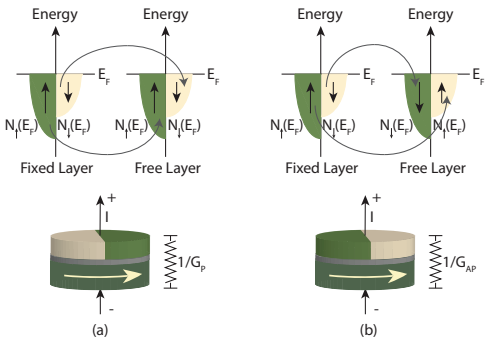


Figure 2.3: Density of states for FM layers in 1 and 0 states. For (a) parallel MTJ; (b) antiparallel MTJ. The net device conductance is proportional to the product of the density of states of the same spin for the fixed and the free layers.

TMR is a subset of the more generalized magnetoresistance (MR=Δ G/G) effect. When tunneling occurs across the barrier between the FM electrodes, as in MTJs, the phenomenon is called TMR. Interestingly the first MR phenomenon was discovered in 1856 [22, 38], but it was not until 1975 that Julliere [39] first defined it on a $Fe/Ge/Co$ junction (Eq. 2.3).

$$\Delta G/G = 2P_1P_2/(1 - P_1P_2) \tag{2.3}$$

where, $P_{1,2}$ are the spin polarization factors for the two FM electrodes [19, 22]

$$P_i = [N_\uparrow(E_F) - N_\downarrow(E_F)]/[N_\uparrow(E_F) + N_\downarrow(E_F)] \tag{2.4}$$

Julliere observed a MR ratio of 14% at 4.2K, which was not sufficient for any commercial application. Later experiments with different junction materials have helped to improve the MR (see Table 2.1).

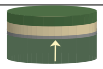
Table 2.1: MR improvement over the years.

Year	Device Junction	MR value @ temperature
Julliere[39], 1975	Fe/Ge/Co	14% @ 4.2K
Miyazaki et al.[40], 1995	$Fe/Al_2O_3/Fe$	18% @ RT*
Bowen et al.[41], 2001	Fe(001)/MgO/FeCo(001)	27% @ RT
Kano et al.[42], 2002	$CoFeB/Al_2O_3/FeCo$	59.5% @ RT
Parkin et al.[24], 2004	$(Co_{70}Fe_{30})_{80}B_{20}/MgO/Co_{70}Fe_{30}$	220% @ RT
Yuasa et al.[43], 2006	Co(001)/MgO(001)/Co(001)	410% @ RT
Wang et al.[44], 2009	$Co_2FeAl_{30}/MgO/Co_{75}Fe_{25}$	700% @ 10K

2.2.3 MTJ Types

Depending on the plane of polarization of the free and the fixed layer, we have categorized MTJs into three types. Table 2.2 defines them, their properties, tradeoffs and applications.

Table 2.2: MTJ types.

Type	Definition	Figure	Pros	Cons	Applications
i-MTJ	FL*: inplane; RL†: inplane		TMR: high	I_{sw}‡: high	Memory
p-MTJ	FL: out-of-plane; RL: out-of-plane		TMR: med	I_{sw}: low	Memory
t-MTJ	FL: inplane; RL: tilted		TMR: low	I_{sw}: med	Oscillator

*FL: Free layer, †RL: Reference layer or Fixed layer, ‡I_{sw}: Switching current.

2.2.4 Spin Transfer Torque

Spin transfer torque (STT) originates when the spin of conduction electrons interacts with the local magnetic moment of a material [26, 45]. By transferring a part of their angular momentum to the magnet, the electrons directly apply a torque on the magnet. Exchange interactions rather than current induced magnetic fields are responsible for this

torque. With sufficient current, the torque can stimulate magnetic excitation or reverse the magnetization in the material.

STT is used in MTJs to switch the free layer. In MTJs, when a stream of electrons flow from the fixed to the free layer, majority gets oriented in the direction of the magnetic moment of the fixed layer by the time they leave the fixed layer. On reaching the free layer, they transfer their angular momentum, which results in a spin torque on the free layer trying to drive it to the parallel state [45] (see Fig. 2.4a). On the other hand, when a stream of electrons flow from the fixed to the free layer, they first get polarized by the free layer. When they strike the fixed layer only the ones with the same polarization as the fixed layer move through it. Electrons with opposite polarization get reflected and now exert a torque on the free layer that tends to drive it to the antiparallel state (see Fig. 2.4b). When the torque magnitudes are above a critical value, the free layer switches.

The equation governing the magnetodynamics of the free layer is given by Eq. 2.5.

$$\frac{d\mathbf{M}}{dt} = -\gamma \mathbf{M} \times \mathbf{H_{eff}} + \frac{\alpha}{M_s}\mathbf{M} \times \frac{d\mathbf{M}}{dt} + \frac{\gamma J_e G}{J_p}\mathbf{M} \times \mathbf{e_p} \times \mathbf{M} \tag{2.5}$$

where, J_e is the current density through the MTJ and

$$G = \left[-4 + (1+P)^3 \frac{(3 + \hat{s_1}.\hat{s_2})}{4P^{3/2}}\right]^{-1} \tag{2.6}$$

$$J_p = \mu_0 \cdot M_s \frac{\mid e \mid t_F}{\gamma \hbar} \tag{2.7}$$

Table 2.3 defines the symbols. The first term on the right hand side of Eq. 2.5 defines the precession (τ_H), the second term defines the damping (τ_d) and the third term defines the spin torque (τ_{st}). During a write 0 the damping acts in the same direction as spin torque while during a write 1 the damping opposes the spin torque (see Fig. 2.5). Therefore current to write 0 is lesser than current to write 1. The critical write current I_{crit} to write the MTJ

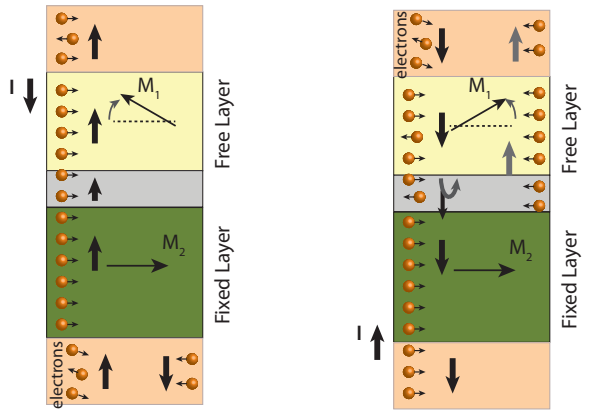


Figure 2.4: Theory of spin torque. Electrons flowing from the (a) fixed to the free layer exerts spin transfer torque on the free layer that tends to drive it to the parallel state; (b) free to fixed layer gets reflected from the boundary of fixed layer and exerts a torque on the free layer that tends to drive it to the antiparallel state.

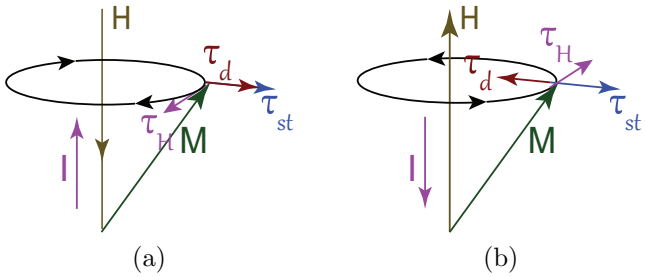


Figure 2.5: Torques on free layer during (a) write 0; (b) write 1.

is given by [46], where ± is to write a 1 or 0. Note that the current I_{crit} scales with MTJ volume V.

$$I_{crit} = \frac{2e\alpha M_s V(H_K \pm H_{ext} + 2\pi M_s)}{\hbar\eta} \tag{2.8}$$

2.3 Nanomagnetic Logic

2.3.1 Fundamental Concepts

Nanomagnetic logic (NML) is a post-CMOS computing technology involving dipolar coupling between nanomagnets. The nanomagnets are sized for their single-domain behavior (see Fig. 2.6a). For lithographic limitations, most of the NML studies are conducted with

Table 2.3: Symbol definitions.

Symbol	Description
a	Aspect ratio of the cell.
α	Gilbert damping constant.
d	Separation between cells.
e	Electron charge.
$\mathbf{e_p}$	Unit vector for magnetization along fixed layer.
η	Spin transfer efficiency.
γ	Gyromagnetic ratio.
$\mathbf{h_{eff}}$	Unit vector along effective magnetic field on the free layer arising. from crystalline and shape anisotropy, demagnetization field, exchange field and external field including coupling from the fixed layer.
H_K	Effective anisotropy field including magnetocrystalline anisotropy. and shape anisotropy.
$\hbar$	Reduced Planck's constant.
K_U	Anisotropy constant.
$\mathbf{m_1}$, $\mathbf{m_2}$	Unit vectors in direction of magnetization of free and fixed layer.
M_s	Saturation Magnetization.
μ_0	Permeability of free space.
$\mathbf{N}$	Demagnetization tensor.
P	Spin polarizing factor.
r	Radius of clock wire.
$\hat{s_1}$, $\hat{s_2}$	Unit vectors along the global spin orientation of the free and fixed layers.
t_F	Thickness of free layer.
V	Volume of free layer.

single-domain nanomagnets around 100nm in width and an aspect ratio of 2 [47, 48, 49]. A spacing of 20nm is typically chosen between nanomagnets to ensure effective dipolar coupling.

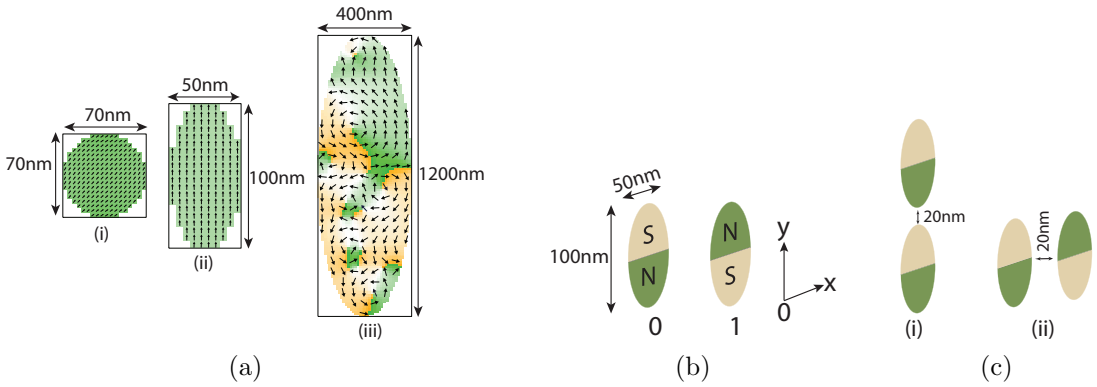


Figure 2.6: Domains, logic states and coupling in nanomagnets. (a) (i) Single-domain circular nanomagnet; (ii) Single-domain elliptical nanomagnet; (iii) Multiple-domain nanomagnet (Not drawn to scale). The simulations are carried out using Object Oriented MicroMagnetic Framework (OOMMF) [50]. (b) NML logic states. (c) Coupling between 20nm spaced nanomagnets: (i) Ferromagnetic coupling; (ii) Antiferromagnetic coupling.

Just like MTJs, the aspect ratio gives a shape anisotropy that generates two stable magnetization states along the easy axis at room temperature [51, 52]. The two states are used to represent 1 and 0 in logic. The two stable states are separated by an energy barrier, which is an unstable magnetization state and is also called the hard axis of the nanomagnet. Another important property of nanomagnets is their remanence, which is best explained by their hysteresis loop (see Fig. 2.7a). When there are no external magnetic fields acting on the nanomagnet, it continues to retain its previous state (position A and C in Fig. 2.7a). This accounts for the non-volatile behavior of NML.

2.3.2 Logic and Interconnects

When two single-domain nanomagnets are placed around 20nm apart, they experience dipolar coupling. There are two types of coupling: (i) Ferromagnetic; and (ii) Antiferromagnetic. Two nanomagnets with their easy axis aligned will experience ferromagnetic

coupling (see Fig. 2.6c(i)) and with their easy axis in parallel will experience antiferromagnetic coupling (see Fig. 2.6c(ii)). Antiferromagnetic coupling functions as an inverter while ferromagnetic coupling functions as a buffer. Any logic function can be realized by combining the ferromagnetic and the antiferromagnetic coupling [51, 53].

Fig. 2.7b shows a 3-input majority voter Y = A·B + B·C + C·A. The output equals the majority of inputs through a series of ferromagnetic and antiferromagnetic coupling. Y_1, Y_2 and Y_3 are the intermediary cells. In Fig. 2.7b we have worked out the logic for different input combinations. When A=1(0) the majority behaves as a 2-input OR(AND). Together with the inverter (Fig. 2.6c (ii)), the majority forms the universal minority function [54].

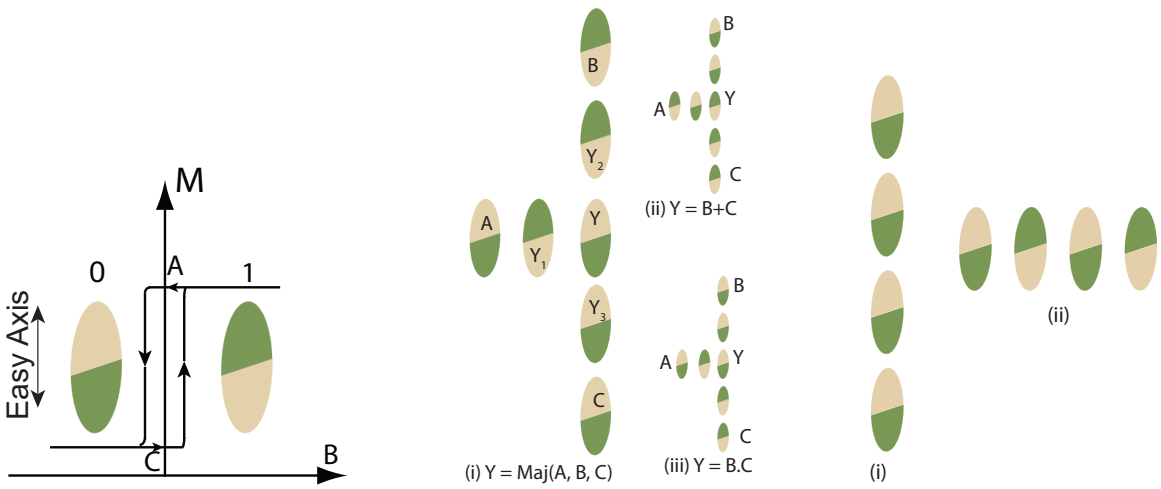


Figure 2.7: Magnetic hysteresis and majority voter. (a) Hysteresis in nanomagnets; (b) Majority voter, Y = M(A, B, C) = A.B + B.C + C.A. (i) Y = M(0, 1, 0) = 0 (ii) M(1, 0, 1) = B+C = 1 (iii) M(0, 0, 1) = B.C = 0. (c) (i) Ferromagnetic; and (ii) Antiferromagnetic wire.

Unlike logic, interconnects require only ferromagnetic or antiferromagnetic coupling (see Fig. 2.7c) [48]. Another interesting feature in NML is the crosswire formed of ferromagnetic coupling [49] where information can flow in orthogonal directions in a single plane. All these logic gates and wires have already been experimentally demonstrated [48, 49, 51, 55].

2.3.3 Clock

The logic states in nanomagnets are separated by an energy barrier E_b. For a single-domain nanomagnet with uniaxial anisotropy, E_b is given by Eq. 2.9 [56].

$$E_b = \left(K_U + \frac{\mu_0 M_s^2 (1 - 3D)}{4} \right) V \tag{2.9}$$

where symbols are explained in Table 2.3. For an elliptical cross-section, the demagnetization factor D is roughly given by Eq. 2.10, where a is the aspect ratio and is > 1.

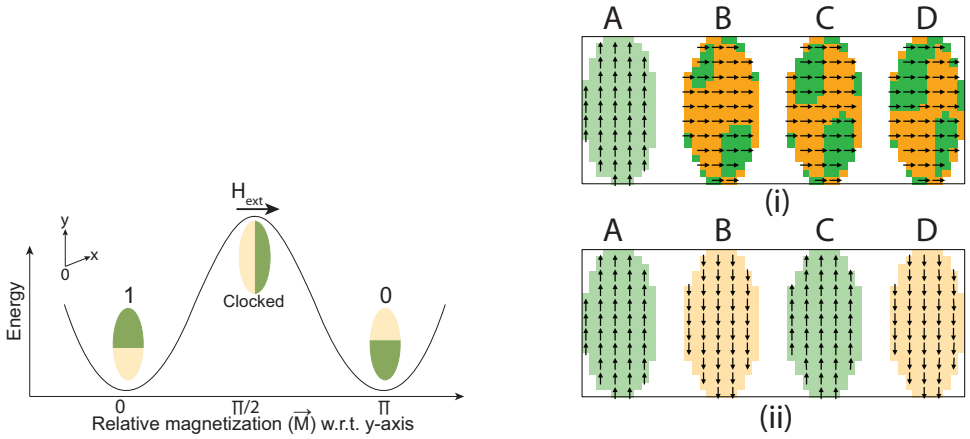
$$D = \frac{1}{2a + 1} \tag{2.10}$$

For reasonable error probability $e^{-(E_b/k_B T)} < e^{-30}$, which means $E_b \geq 30 k_B T$ [57]. For nanomagnet dimensions of $100 \times 50 \times 2$ nm^3, the energy barrier $E_b \approx K_U \ V > 1200 \ k_B T$. This ensures the stability of logic states at room temperature. However, when we want to compute we want the nanomagnets to couple and settle for their new ground states. The dipole-dipole interaction energy of nanomagnets is given by Eq. 2.11 [57]. For ferromagnetic and antiferromagnetic coupling, the coupling energy is given by Eq. 2.12.

$$E^{i-j}_{dipole-dipole} = \frac{\mu_0 M_s^2 V^2}{4\pi |\overrightarrow{d}_{i-j}|^3} \left[\overrightarrow{m}_i \cdot \overrightarrow{m}_j - \frac{3}{|\overrightarrow{d}_{i-j}|^2} (\overrightarrow{m}_i \cdot \overrightarrow{d}_{i-j})(\overrightarrow{m}_i \cdot \overrightarrow{d}_{i-j}) \right] \tag{2.11}$$

$$E_{dipole-dipole} = \frac{\mu_0 M_s^2 V^2}{4\pi d^3} \tag{2.12}$$

For $100 \times 50 \times 2 \text{nm}^3$ nanomagnets with 20nm spacing the ferromagnetic and antiferromagnetic coupling energies are $0.896 k_B T$ and $4.48 k_B T$, none of which are sufficient to flip the state of the nanomagnets. Therefore to compute with nanomagnets, we need an extra force that can help to cross the barrier but not impact the direction of crossing the barrier. In practice we need a force that takes the nanomagnets to their hard axis from where coupling takes over.



(a) (b)

Figure 2.8: Energy landscape and clock. (a) Energy landscape in nanomagnets; (b) (i) t = 0 state of a clocked antiferromagnetic wire. A is the input while B, C, D are clocked; (ii) final state of the wire after clock is released. The simulations were run using OOMMF software.

In NML this is called the clock, which is an external field directed along the hard axis of nanomagnets (see Fig. 2.8a(a)) in order to destabilize them. When the clock is released, the nanomagnets reorient according to the coupling from their neighbors (see Fig. 2.8b).

The early implementations of clock were slowly increasing external fields also called pumping fields directed along the hard axis of the nanomagnets. These fields were then slowly reduced to zero. If the pumping process is slow enough, typically in MHz, the switching becomes adiabatic in nature [58]. More recently an on-chip clock field generation scheme was introduced [59] where copper wires cladded with ferromagnetic wires were used. The wires were placed underneath the nanomagnets and could clock 100-1000 nanomagnets together. The required clock field H_{req}, current density J_{clk} and nanomagnet dimensions V are related by Eq. 2.13, where r is the radius of the wire [57].

$$H_{req} = \frac{E_b}{\mu_0 M_s V} = \frac{J_{clk} r}{2} \tag{2.13}$$

For a nanomagnet of dimension $100 \times 50 \times 2\text{nm}^3$ and a clock wire of radius 200nm the clocking current is 10mA. To reduce the clocking current, clocking structure with enhanced

permeability dielectric (EPD) films surrounding the dielectric has been proposed [60]. Apart from high clocking current some other drawbacks of this field induced clock are: (i) non-scalability of clock current $J_{clk} \propto 1/V$; and (ii) no cell selectivity or individual nanomagnets cannot be selected from a group for clocking. More recently researchers have proposed and demonstrated the use of strong localized in-plane magnetic fields generated by domain walls superposed with externally applied fields for clocking and switching nanomagnets [61, 62]. For a $200ms^{-1}$ propagating domain wall, a current density of $2 \times 10^{12}Am^{-2}$ is required [63], which is equivalent to a current of 3.6mA for a typical $100 \times 18nm^2$ domain wall conductor. The current requirements for clocking are therefore still high.

2.3.4 Inputs and Outputs

Initially off-chip standard moment magnetic force microscopy (MFM) probe was used to write and read from NML [49]. Based on simulation results on-chip writing technique using fields generated by the free layer of MTJs have been proposed [64]. Possible reading techniques have also been proposed using inductive methods, capacitive methods and MTJs [23]. Recently MTJ based magnetoresistive read of single-layer nanomagnets [65] has been experimentally demonstrated. Other possible writing techniques involve keeping the ferromagnet in contact to a multiferroic layer and applying an electric field to the ferromagnet/multiferroic heterostructure [66].

2.3.5 Concerns

Some of the concerns of NML include:

(i) mA range clocking current;

(ii) non-scalability of clock;

(iii) lack of reliable on-chip read and write techniques;

(iv) lack of selectivity over logic cells;

(v) lack of CMOS user interface for on-chip automation;

(vi) random and repeatable errors in nanomagnet chains from process variations [67].

2.4 Conclusion

In this chapter we have discussed STT-MRAM and the key properties of MTJs. We studied the MTJ structure and the concept of TMR. Thereafter we studied the theory of STT and the mechanism of STT based write in MTJs. Next we discussed NML, a post-CMOS magnetic dipolar-coupling based non-volatile logic technology. We described the elemental logic cells and the two types of coupling. We then discussed the fundamentals of coupling based computation and the necessity of clocking. We concluded this chapter with some of the concerns of NML. In the next chapters we will describe the ways we have married the two technologies to demonstrate the ability of STT-MRAM in unconventional roles for modern computing devices.

CHAPTER 3

STT-MRAM BASED LOGIC-IN-MEMORY ARCHITECTURE

3.1 Introduction

In the last chapter we studied some of the properties of STT-MRAM that makes it one of the promising non-volatile memory technologies of today. In this chapter we will discuss how some of these properties can be used to extend the role of STT-MRAM into computing. As we discussed in Section 2.2, the elemental cell of STT-MRAM is magnetic and is monolithically integrated to CMOS. It can be written with the help of STT and can be read with the help of TMR. We have also discussed under Section 2.3 a post-CMOS zero-leakage magnetic logic technology that uses dipolar coupling between magnetic cells to compute logic. In this chapter we will discuss how STT-MRAM technology can readily import some of the NML concepts. We have then used this property to design a sustainable non-volatile logic-in-memory platform.

Such a non-volatile platform or architecture as we will interchangeably call in this dissertation can help to save several initialization cycles in CPU [68]. It can also help to reduce leakage and aid in fine grain power gating [69, 70]. Such power savings are critical for sustainable computing and battery powered platforms. The savings in leakage becomes even more significant at high temperatures that are common in automobiles. In this non-volatile logic-in-memory architecture we have used NML style for computation and STT-MRAM style for

[0]This chapter was published in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 59(9): pp. 2008-2016, 2012, "Ultra-low Power Hybrid CMOS-Magnetic Logic Architecture", Jayita Das, Syed M Alam, and Sanjukta Bhanja. Permission attached in Appendix A and
11th IEEE Conference on Nanotechnology (IEEE-NANO), pp. 1261-1266, 2011, " Low power cmos-magnetic nano-logic with increased bit controllability", Jayita Das, Syed M Alam, and Sanjukta Bhanja. Permission attached in Appendix A.

read and write. For clock we have used a new style that we have discussed in Chapter 4. In this chapter we have discussed the design challenges of the architecture, the key features, the elementary cell types and the operation techniques of the architecture. In the next section we will briefly review some existing non-volatile MTJ based logic for completeness before going into the architecture details.

3.2 Previous Work

Wang et al. in 2005 [71] demonstrated 2-input non-volatile logic functions based on magnetic field and thermally induced switching of MTJs. AND, OR, NOR, NAND, XOR, XNOR were demonstrated. Their main drawbacks were high currents of around 70mA and low MR of around 14%. Ikeda et al. developed 2-input logic functions by a parallel combination of MTJs and CMOS transistors [72]. In the logic one input was stored in the MTJs and the other was directly applied to the CMOS transistors. Here the MR of MTJs were used to calculate the logic output. Matsunaga et al. demonstrated 3-input circuits like MTJ based full adders in 2008 [73]. Researchers have also explored non-volatile programmable logic functions using MTJ/CMOS based LUTs [17, 74, 75]. However, none to our knowledge have used dipolar coupling between MTJs for logic computation.

3.3 Theory of STT-MRAM Based Logic Architecture

As we discussed in Section 2.2.1, the free layer and the fixed layer in MTJs are ferromagnetic and single-domain. However, only the free layer can switch. When MTJs are within 20nm of one another their free layers can also couple. The coupling can be either ferromagnetic or antiferromagnetic (see Fig. 2.6c). We have also validated the coupling through simulations and fabrications [76, 77]. Here we have used this coupling between free layers to design our computing platform [78, 79]. Our chosen MTJ dimensions are $100 \times 50\text{nm}^2$ and their spacing is 20nm. This is also the same as in NML.

Just like single-layered nanomagnets the MTJs are patterned with a shape anisotropy. As a result the ground states in their free layers are separated by an energy barrier E_b, which determines their thermal stability or bit stability at room temperature. As we have seen in Section 2.3.3, an $E_b \geq 30k_BT$ is required to maintain high bit stability. We have also seen that the energy from coupling is not sufficient to help a magnet to cross over the barrier. Therefore, like NML a clock signal is required to assist coupling based computation in MTJs. The clock can be an external magnetic field directed along the hard axis of MTJs. However, as we have seen in Section 2.3.3 a field based clock requires high current and is not scalable. To build a sustainable computing platform we therefore need a low power clock. In Section 4.2 we have proposed a novel spin transfer torque (STT) based clock for MTJs. The clock current is much lesser than field-induced clock. It is also scalable. Like in memory we have used STT to write inputs into the architecture (Section 4.3). In Section 2.2.2 we have already studied the phenomenon of TMR and in Section 4.4 we have proposed a on-chip variability tolerant TMR based differential read scheme for the architecture. The TMR based read scheme is also low power. Finally with CMOS integration we aim to achieve fine-grain selection of cells, which can reduce the random errors in nanomagnetic chain [80].

3.4 Design Challenges

The design challenges for the architecture arose from the need to fulfill the conflicting technical requirements discussed below:

(i) A regular cell layout;

(ii) Cell size between thermal stability and single-domain limits;

(iii) Maximum integration of access transistors;

(iv) 20nm spacing between MTJs;

(v) Metal pitch of CMOS technology;

(vi) Sufficient drive capability of access transistors; and

(vii) Minimum metal layers for low cost implementation.

We resolved the challenges by [81, 82]:

(i) Choosing $100 \times 50\text{nm}^2$ cross-section cells;

(ii) Selecting 22nm CMOS technology node;

(iii) Integrating one access transistors for every 2×2 STT-MRAM cell arrays (see Fig. 3.1a).

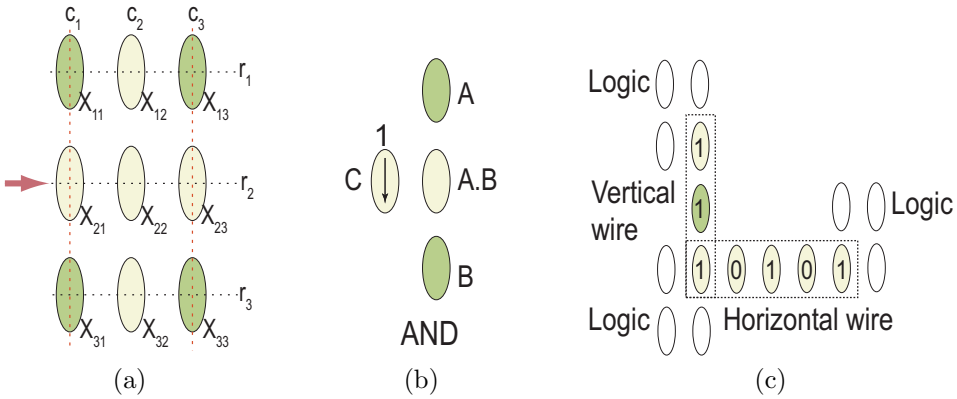
Table 3.1 compiles the design rules for the architecture.

Table 3.1: Design rules of the architecture.

Parameters	Design Rule
Cell cross-section	$100 \times 50\text{nm}^2$
Row pitch	70nm
Column pitch	120nm
Access transistor	one every 2×2 array

3.5 CMOS Integration

Fig. 3.1a shows the integration of access transistors. Only alternate MTJs in a row or column can have access transistor. The architecture is regular with three layers of metal like memory. Fig. 3.1b and Fig. 3.1c shows logic gates and cell interconnects in the architecture. Fig. 3.2 shows a cross-section of the architecture along column c_1 of Fig. 3.1a. The sourcelines and bitlines are in metal M1 and M2 respectively. They run parallel to the rows. The wordlines are in metal M3 (see Fig. 3.3a). They run parallel to the columns. The sourcelines are either connected to the source of access transistors (e.g. X_{11}) or to the fixed layer of MTJs that are without access transistors (e.g. X_{12}). The bitlines are connected to the free layer of MTJs. The wordlines are connected to the gates of the access transistors. Table 3.2 summarizes the metal pitch in the architecture and the CMOS 22nm technology



(a) (b) (c)

Figure 3.1: Architecture layouts. (a) The regular architecture layout with green MTJs integrated with access transistor and yellow MTJs without access transistors. (b) MTJ layouts for two-input AND. Cell C is fixed to 1. (c) Vertical and horizontal wires. (© 2012 IEEE, with permission.)

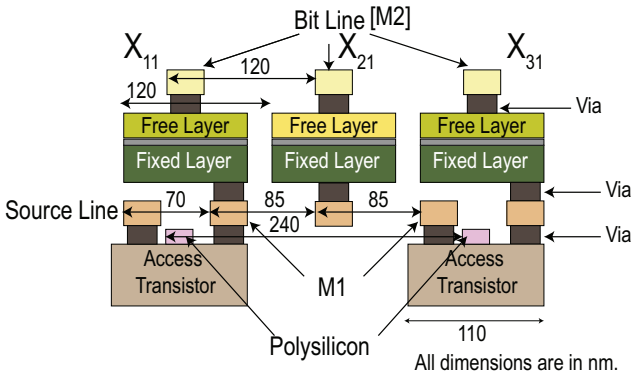


Figure 3.2: A cross-section of a column. (© 2012 IEEE, with permission.)

requirements. Fig. 3.3a shows a 3D view of a column and Fig. 3.3b shows a 3D view of a row in the architecture.

To summarize, the salient design features of the architecture are:

(i) It is regular;

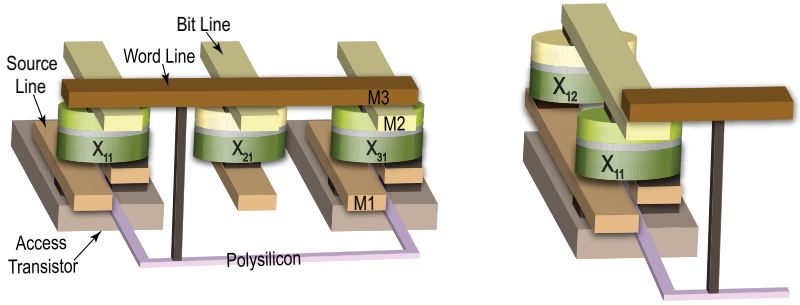
(ii) An access transistor for every 2×2 MTJ array;

(iii) Three layers of metal lines operating the cells;

(iv) A sourceline and bitline for every row and a wordline for every alternate column.

Table 3.2: Metal pitch in the architecture. (© 2012 IEEE, with permission.)

Metal Layer	Control Line	Architecture Pitch	Required $22nm$ CMOS pitch [83]
Metal 1	Sourceline	70nm	64nm
Metal 2	Bitline	120nm	$>$ 64nm
Metal 3	Wordline	140nm	$>$ 64nm



(a) (b)

Figure 3.3: 3D view of (a) a column; (b) a row. (© 2012 IEEE, with permission.)

3.6 Operation Techniques of the Architecture

The MTJs in the architecture are to be written or clocked with STT. We have already discussed the theory of STT write in Section 2.2.4 and we will be discussing the theory of STT clock in Section 4.2. In this section we will briefly discuss the CMOS operations during write and clock. The write technique is very similar to STT-MRAM. Only MTJs with access transistors are to be written. During write the required potential is to be applied across the bitline and sourceline of the MTJ to be written and the corresponding wordline needs to be activated. Clocking is similar. The appropriate potential is to be applied across the bitline and sourceline of the MTJs and corresponding wordlines (if present) need to be activated.

3.7 Cell Types

We have divided the architecture cells into three broad types based on their responsibilities. With the help of the layout of a 2-input XOR (see Fig. 3.4), we have explained the cell functions and their placements in the architecture.

(i) Input Cells: These MTJs are the inputs to logic gates and are only written. They should always have access transistors and are never clocked. A, B , ¬A and ¬B are the input cells in Fig. 3.4. They are marked in pink.

(ii) Output Cells: These MTJs hold the outputs of logic. They have access transistors and are both clocked and read. The output cells in Fig. 3.4 are marked in orange.

(iii) Logic Cells: These MTJs form the body of logic and the actual computation takes place in these cells. These MTJs are only clocked and are never written nor read. We have further classified them into:

(a) Standard Cells: These cells are without access transistors (marked in yellow in Fig. 3.4).

(b) Controlled Cells: These cells are with access transistors (marked in green in Fig. 3.4).

3.8 Elementary Logic Blocks

The three building blocks for logic in this architecture are:

(i) Majority: The 3-input majority layout is similar to NML (see Fig. 2.7b). Along with the inverter it forms the minority, which is a universal logic function [54]. The majority can also be reconfigured to perform 2-input AND/OR operations (see Section 2.3.2) [51].

(ii) Wires: They can be horizontal or vertical.

(a) Horizontal wires: Here the MTJs couple antiferromagnetically. The information propagates through the cells as an alternating pattern of 1s and 0s (see Fig. 3.1*c*).

(b) Vertical wires: Here the MTJs couple ferromagnetically. The information propagates through the cells without alternating (see Fig. 3.1*c*).

(iii) Differential output generator: This generates output, S, and its complement, ¬S, which are used by the read circuit discussed in Section 4.4.

3.9 Case Study: 2-input XOR

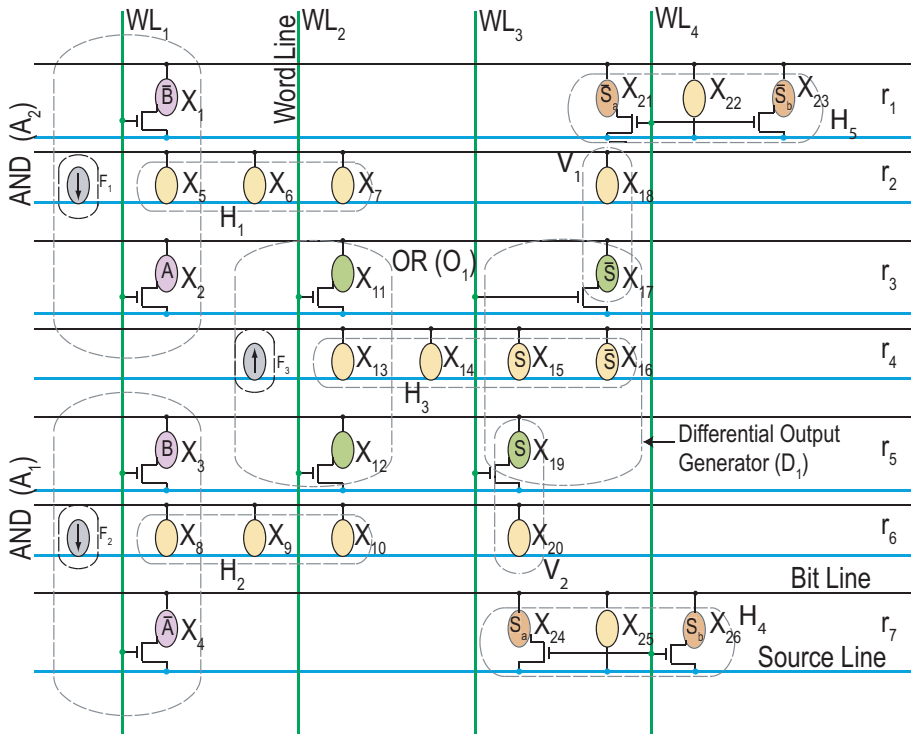


Figure 3.4: Layout of a 2-input XOR. The black and blue horizontal lines are the bitlines and sourcelines. The green vertical lines are the wordlines. (© 2012 IEEE, with permission.)

The layout of a two-input XOR is shown in Fig. 3.4. (i) Input cells are in pink; (ii) Standard cells are in yellow; (iii) Controlled cells are in green; and (iv) Output cells are in orange. (i) The sourcelines are horizontal and are in blue; (ii) the bitlines are horizontal and are in black; and (iii) the wordlines are vertical and are in green.

3.9.1 Layout Description

In Fig. 3.4, the MTJs are placed in a regular array and removed from locations to fulfill logic requirements. The array has one access transistor for every 2×2 MTJ array. To

minimize power, current supply to MTJs should be gated with access transistors. A power efficient design should have more number of controlled cells. X_{11}, X_{12}, X_{17} and X_{19} are the controlled cells and $X_{13} \cdots X_{16}$ are the standard cells. They follow the architecture design rules. The output and its complement are generated in X_{15} and X_{16} and are copied through vertical wires into X_{24}, X_{26} and X_{21}, X_{23}. They are then read out using a differential read. Table 3.3 summarizes the logic blocks and their counts in the 2-input XOR layout. Algorithm 1 outlines the operation sequence for the 2-input XOR.

Table 3.3: Logic blocks in the 2-input XOR layout.

Block Type	Counts	Label
Majority (AND)	Two	A_1, A_2
Majority (OR)	One	O_1
Horizontal Wire	Five	H_1, H_2, H_3, H_4, H_5
Vertical Wire	Two	V_1, V_2
Differential Output Generator	One	D_1

Inputs: A, ¬A, B, ¬B. **Outputs:** $S_a = S_b$ = f(A,B) = A ⊕ B.
Phase I: Write X_1=¬B, X_2=A, X_3=B, X_4=¬A.
Phase II: Clock rows r_2 and r_6.
Phase III: Release clock.
X_5 X_6 and X_7 settle to A.¬B, ¬A.¬B and A.¬B respectively.
X_8 X_9 and X_{10} settle to ¬A.B, ¬(¬A.B) and ¬A.B respectively.
Phase IV: Select wordline WL_2. Clock rows r_3 and r_5.
Phase V: Release clock.
X_{11} and X_{12} settle to A.¬B and ¬A.B respectively.
Phase VI: Clock row r_4.
Phase VII: Release clock. X_{13}, ... X_{16} settle to (A⊕B) ... ¬(A⊕ B) respectively.
Phase VIII: Select wordline WL_3. Clock rows r_3, r_2, r_5 and r_6.
Phase IX: Release clocks in sequence: $r_3 \rightarrow r_2$ and $r_5 \rightarrow r_6$.
Both X_{17} and X_{18} settle to ¬(A⊕B).
Both X_{19} and X_{20} settle to A⊕ B.
Phase X: Select wordline WL_4. Clock rows r_1 and r_7.
Phase XI: Release clock.
X_{21} and X_{23} settle to ¬(A⊕B)=¬S_a and ¬S_b respectively.
X_{24} and X_{26} settle to A⊕B=S_a and S_b respectively.

Algorithm 1: Operation sequence of 2-input XOR. (© 2012 IEEE, with permission.)

3.10 Conclusion

In this chapter we have introduced the first auxiliary role of STT-MRAM. We have discussed the design of a logic-in-memory architecture that can compute with STT-MRAM. In this architecture the STT-MRAM cells are spaced within interacting distance of one another. This new spacing puts a constraint on the metal pitch of the underneath CMOS. Here we have resolved this constraint by selecting 22nm CMOS technology node and integrating access transistors selectively with the MTJs. Depending on the logic responsibilities and the CMOS integration we have further classified the cells in the architecture into input, output and logic. Finally, we have discussed a 2-input XOR layout and its operation sequence.

CHAPTER 4

LOW POWER STT CLOCKING AND I/O INTERFACE

4.1 Introduction

The MTJs are patterned with a shape anisotropy to have two logic states that are separated by an energy barrier E_b at room temperature. This energy barrier helps the MTJs to save their states. When MTJs are brought close to one another, their free layers couple. However, as we have studied in Section 2.3.3, this coupling energy is not sufficient to flip the states of any MTJ. To compute with the help of coupling we need a clock that would assist the coupling without affecting the results. In Section 2.3.3 we have discussed external field based clock for NML. However, the major concerns involved were high current, non-scalability and lack of cell selectivity. In this chapter we have proposed a spin torque based clock that reduces the above three concerns as well as suits the needs and goals of the architecture. In addition we have also discussed the CMOS aided writing and reading.

4.2 Concept of STT Clock

In the multi-layered cells the magnetodynamics of the free layer can be controlled by a spin transfer torque. The magnetodynamics is governed by the LLG equation (Eq. 4.1)

[0]This chapter was published in parts in IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 1(3): pp. 267-276, 2011, "Low Power Magnetic Quantum Cellular Automata Realization Using Magnetic Multi-Layer Structures", Jayita Das, Syed M Alam, and Sanjukta Bhanja. Permission attached in Appendix A, and
IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 59(9): pp. 2008-2016, 2012, "Ultra-low Power Hybrid CMOS-Magnetic Logic Architecture", Jayita Das, Syed M Alam, and Sanjukta Bhanja. Permission attached in Appendix A.

under the fundamental constraint given by Eq. 4.2. The last term in the equation denotes the contribution from spin transfer torque, which was added to the equation in 1996 by Slonczewski [32]. The symbols in the equation are explained in Table 2.3.

$$\frac{d\mathbf{M}}{dt} = -\gamma \mathbf{M} \times \mathbf{H_{eff}} + \frac{\alpha}{M_s}\mathbf{M} \times \frac{d\mathbf{M}}{dt} + \frac{\gamma J_e G}{J_p}\mathbf{M} \times \mathbf{e}_p \times \mathbf{M} \tag{4.1}$$

$$|\mathbf{M}(\mathbf{r}, t)| = M_s \tag{4.2}$$

Fig. 2.5 shows the torques from precession τ_H, damping τ_d and spin transfer τ_{stt} acting on the free layer at any instant. The free layer continues to precess under the influence of the net torque acting on it. An equilibrium will be reached if the net torque acting on the layer is zero, i.e. $\tau_{\mathbf{eff}} = \tau_H + \tau_d + \tau_{stt} = 0$. Once we reach this condition we can reach a state of static magnetization $d\mathbf{M}/dt = 0$. Our next objective is to reach this static state at $\phi = \pm\pi/2$. This would solve our clocking problem. Under static equilibrium Eq. 4.3 is valid.

$$\mathbf{M} \times \mathbf{H_{eff}} = \frac{J_e G}{J_p}\mathbf{M} \times \hat{\mathbf{e}}_\mathbf{p} \times \mathbf{M} \tag{4.3}$$

where $\hat{\mathbf{e}}_\mathbf{p} = \hat{\mathbf{e}}_\mathbf{x}$. The spin-torque clocking is successful if by using appropriate current we can drive the cell to a stationary magnetization state along the y-axis. The clocking current can therefore be theoretically derived from Eq. (4.3) and equating the field components along the $\hat{x}$, $\hat{y}$ and $\hat{z}$ directions [84]. $\mathbf{H_{eff}}$ is given by [31]

$$\mathbf{H_{eff}} = \mathbf{H_a} + \mathbf{H_d} + \mathbf{H_M} + \mathbf{H_{AN}} \tag{4.4}$$

where $\mathbf{H_a} = H_{ax}\hat{\mathbf{e}}_\mathbf{x} + H_{ay}\hat{\mathbf{e}}_\mathbf{y} + H_{az}\hat{\mathbf{e}}_\mathbf{z}$ is an applied field, $\mathbf{H_d} = H_{dx}\hat{\mathbf{e}}_\mathbf{x}$ is the dipolar coupling from the fixed layer, $\mathbf{H_M}$ is the field due to demagnetization effects and $\mathbf{H_{AN}}$ is the field arising from the crystalline and shape anisotropy of the free layer. In the clocked state or $\phi = \pm\pi/2$ state, $\mathbf{H_{AN}} = 0$ and $\mathbf{H_M}$ = -$N_y.M_y.\hat{\mathbf{e}_\mathbf{y}}$ owing to the presence of only the y-

component of magnetization in the free layer. Therefore $\mathbf{H_{eff}}$ in the clocked state is given as follows

$$\mathbf{H_{eff}} = H_{ax}\hat{\mathbf{e}}_\mathbf{x} + H_{ay}\hat{\mathbf{e}}_\mathbf{y} + H_{az}\hat{\mathbf{e}}_\mathbf{z} + H_{dx}\hat{\mathbf{e}}_\mathbf{x} - N_y M_s \hat{\mathbf{e}}_\mathbf{y} \tag{4.5}$$

Also from the fundamental constraint given in Eq. 4.2 and from the clocking requirements, $\mathbf{M}(\mathbf{r}, t)$ is given by Eq. 4.6

$$\mathbf{M}(\mathbf{r}, t) = M_s(0 \cdot \hat{\mathbf{e}}_\mathbf{x} + 1 \cdot \hat{\mathbf{e}}_\mathbf{y} + 0 \cdot \hat{\mathbf{e}}_\mathbf{z}) \tag{4.6}$$

Substituting Eq. 4.5 and Eq. 4.6 in Eq. 4.3, we see that the righthand side has only $\hat{\mathbf{e}}_\mathbf{x}$ component from the product $(\hat{\mathbf{e}}_\mathbf{y} \times \hat{\mathbf{e}}_\mathbf{x} \times \hat{\mathbf{e}}_\mathbf{y})$, while the left hand side has both $\hat{\mathbf{e}}_\mathbf{x}$ and $\hat{\mathbf{e}}_\mathbf{z}$ components from $(\hat{\mathbf{e}}_\mathbf{y} \times \hat{\mathbf{e}}_\mathbf{x})$ and $(\hat{\mathbf{e}}_\mathbf{y} \times \hat{\mathbf{e}}_\mathbf{z})$ respectively. In the $\hat{\mathbf{e}}_\mathbf{z}$ component arising from $M_s\hat{\mathbf{e}}_\mathbf{y} \times (H_{ax} + H_{dx})\,\hat{\mathbf{e}}_\mathbf{x}$, H_{dx} is a property of the multi-layer and only H_{ax} is user-controlled. This $\hat{\mathbf{e}}_\mathbf{z}$ term on the left hand side can be balanced by the right hand side if $\hat{\mathbf{e}}_\mathbf{p} = \alpha_p\hat{\mathbf{e}}_\mathbf{x} + \gamma_p\hat{\mathbf{e}}_\mathbf{z}$, i.e. if the fixed layer is polarized in the x-z plane and $\alpha_p^2 + \gamma_p^2 = 1$. In this case the new $\mathbf{H_d}$ will be given by

$$\mathbf{H_d} = H_d\alpha_p\hat{\mathbf{e}}_\mathbf{x} + H_d\gamma_p\hat{\mathbf{e}}_\mathbf{z} \tag{4.7}$$

Substituting Eq. 4.7 into Eq. 4.5 we get

$$\mathbf{H_{eff}} = (H_{ax} + H_d\alpha_p)\,\hat{\mathbf{e}}_\mathbf{x} + (H_{ay} - N_y M_s)\,\hat{\mathbf{e}}_\mathbf{y} + (H_{az} + H_d\gamma_p)\,\hat{\mathbf{e}}_\mathbf{z} \tag{4.8}$$

Substituting Eq. 4.8 and the new $\hat{\mathbf{e}}_\mathbf{p} = \alpha_p\hat{\mathbf{e}}_\mathbf{x} + \gamma_p\hat{\mathbf{e}}_\mathbf{z}$ into Eq. 4.3 we obtain the two equalities that need to be satisfied.

$$H_{ax} + H_d\alpha_p = \frac{J_e G\gamma_p M_s}{J_p} \tag{4.9}$$

$$H_{az} + H_d\gamma_p = \frac{J_e G\alpha_p M_s}{J_p} \tag{4.10}$$

Now consider the case $\mathbf{H_a} = 0$, i.e. no external field is applied. Then from Eq. 4.10, $\frac{\alpha_p}{\gamma_p} = \frac{\gamma_p}{\alpha_p}$, which implies $\alpha_p = \gamma_p = \frac{1}{\sqrt{2}}$.

Therefore to realize STT clocking where the clocked state is given by Eq. 4.6, the fixed layer of the MTJ should have a 45° tilt in the $x-z$ plane. In Section 2.2.3 we have seen that such MTJs are already used in oscillators. Substituting the values of G and J_p from Eq. 2.6 and Eq. 2.7, STT clocking current is given by Eq. 4.11.

$$I_{stt-clk} = \left(\frac{\mu_0 \cdot M_s \cdot \mid e \mid \cdot V \cdot H_d}{\hbar \cdot G} \right) \tag{4.11}$$

With a reference layer coupling field of 2500A/m [85], a clocking current of 170μA can be obtained for our MTJ dimensions. This value is also much lower than the clocking current required with magnetic field. Also, the current scales with MTJ dimensions.

4.3 Spin Transfer Torque Write

In Section 3.7 we have categorized the cells of the architecture into Input, Logic and Output depending on their functions. As the name suggests, the Input cells are the ones into which the inputs are written. They were chosen from among cells that have access transistors. Fig. 4.1 shows an Input cell in our logic-in-memory architecture. Here we have borrowed the spin transfer torque (STT) write concept from memory to write inputs of the logic. The motivation behind using spin transfer torque write are:

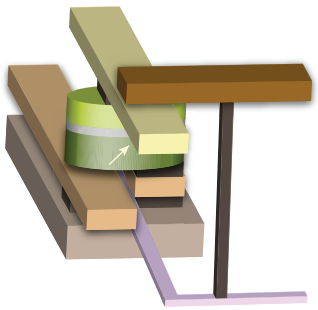


Figure 4.1: Input cell in logic-in-memory architecture. (© 2012 IEEE, with permission.)

(i) Low power compared to field driven write;

(ii) CMOS operability and portability;

(iii) Scalability.

Writing an input in the architecture is a two step process:

(i) Applying the right potential ($V_w > V_{crit}$) across the sourceline and bitline of the Input cell for a duration ($\tau > \tau_{crit}$);

(ii) Activating the wordline of the Input cell for the duration of the write.

The value of V_{crit} can be obtained from the critical write current I_{crit} and the MTJ resistance to be written. V_{crit} trades off inversely with τ_{crit} [16] (Eq. 4.16), giving the designer a choice between low power and high speed operations. The critical write current I_{crit} is given by Eq. 4.12, where we added the $\sqrt{2}$ term in the denominator to take care of the field from tilted polarized fixed layer.

$$I_{crit} = \pm \left(\frac{2e}{\hbar}\right) \left(\frac{\alpha M_s.V}{\eta(\theta)}\right) \left(H_k + \frac{H_{eff}}{2\sqrt{2}}\right) \tag{4.12}$$

The + sign is for current flowing from fixed to free layer and switches the cell to 1 state. The − sign is for current that flows from free to fixed layer and switches the cell to 0 state. The symbols in Eq. 4.12 are defined in Table 2.3.

$$\eta(\theta) = \frac{p}{1 \pm p^2} \tag{4.13}$$

with + sign for switching to 1 state and − sign for switching to 0 state. The other variables in Eq. 4.13 are defined as follows.

$$p = \frac{TMR}{TMR + 2} \tag{4.14}$$

$$H_{eff} = 4\pi M_s \tag{4.15}$$

When the write current I_{sw} exceeds the critical current I_{crit}, the MTJ switches. The physics behind the mechanism of spin transfer torque based switching is already discussed in Section 2.2.4. The current magnitude I_{sw} and the critical pulse width τ_{crit} are related by Eq. 4.16, where θ_0 is the initial angular deviation of the free layer from the hard axis. At 300K, a typical value for standard deviation is $\bar{\theta_0} = 7.7°$ for i-MTJs [86].

$$\tau_{crit} = \frac{1}{(\alpha\mu_0\gamma M_s)} \frac{I_{crit}}{(I_{sw} - I_{crit})} ln\left(\frac{\pi}{2\theta_0}\right) \tag{4.16}$$

$$\theta_0 = \sqrt{\frac{k_B T}{H_c \mu_0 M_s V}} \tag{4.17}$$

From Eq. 4.12 we see that the critical switching current is proportional to the cell volume V. Therefore, as the cell dimensions decrease the critical current also scales down in proportion. This is in contrary to field based switching where the critical current to generate the required magnetic field scales inversely with the volume (see Section 2.3.3). Table 4.1 compares the performance of STT write against field-induced write.

Table 4.1: Comparison between STT write and field based write.

	STT write	Field induced write
I_{avg}	$250\mu A$ [82]	$1.2mA$ [87]
τ_{crit}	$< 3ns$ [88]	$3ns$ [87]
I_{sw}	$\propto$ Volume	$\propto 1/$Volume
Cell selectivity	Yes	No

4.4 TMR Based Differential Read

4.4.1 Motivation

As we already discussed in Section 2.2.2, the TMR distinguishes the resistances between the 0 and 1 states of the MTJs and is given by Eq. 4.18.

$$TMR = \frac{R_1 - R_0}{R_0} = \frac{G_0 - G_1}{G_1} = \frac{\Delta G}{G_1} \tag{4.18}$$

where G_0 and G_1 are the conductances of a MTJ in 0 and 1 state respectively. CMOS integration and TMR together provide for an on-chip electrical readout mechanism for STT-MRAM technology. The conductance G of a MTJ as a function of the angle θ between the magnetization of the free and fixed layers is given by Eq. 4.19 [89].

$$G(\theta) = \frac{1}{2}(1 + cos(\theta))G_P + \frac{1}{2}(1 - cos(\theta))G_{AP} \tag{4.19}$$

where θ as a function of current I through the device is given by

$$\theta \sim cos^{-1}\left[\frac{H_{dz} - \left(\frac{\hbar}{2e\alpha}\right)\left[\frac{g(\pi/2)}{M_s \cdot Vol}\right] I}{4\pi M_s + (H_k \pm H_{dx})/2}\right] \tag{4.20}$$

In our logic-in-memory architecture the cells have a tilted polarized fixed layer, a condition necessitated by low power STT clocking. From Eq. 4.19, it is clear that for t-MTJs, $G_0 < G_P$ and $G_1 < G_{AP}$. Therefore, the value Δ G < (G_P - G_{AP}) is lower than i-MTJs [90]. A lower ΔG sacrifices on the sense margin and requires a higher resolution sense amplifier for reading. The situation becomes more demanding with variabilities in MTJs. Our motivation behind this differential read circuit stems from solving the challenges of (i) reduced ΔG in t-MTJs; and (ii) variabilities in MTJs with the help of available architecture characteristics like (i) complementary output states; and (ii) access transistors with Output cells.

To improve the sense margin here we have proposed reading an Output cell by comparing against its complement rather than a reference, which is the conventional practice in memory (see Section 2.2.2). In doing so we have also saved the costs of maintaining a precise reference at the midpoint of 0 and 1 resistance values as is done in memory.

4.4.2 Variability Tolerant Differential Read

Like any nanoscale processes MTJs are also subjected to variations that affect their electrical properties [91]. One of the common techniques to design variation tolerant circuits

is to include redundancies [92]. Here we have adopted a similar technique where pairs of output cells are read instead of a single cell. In our variation tolerant read circuit, a pair of outputs is compared against a pair of complements [82, 93]. Apart from tolerance to variations, this redundancy also helps to improve the sense margin. However, the tradeoff is in terms of area. Generating the output and its complement in pairs is readily supported by the coupling between the cells in the architecture.

4.4.3 Operation Principle

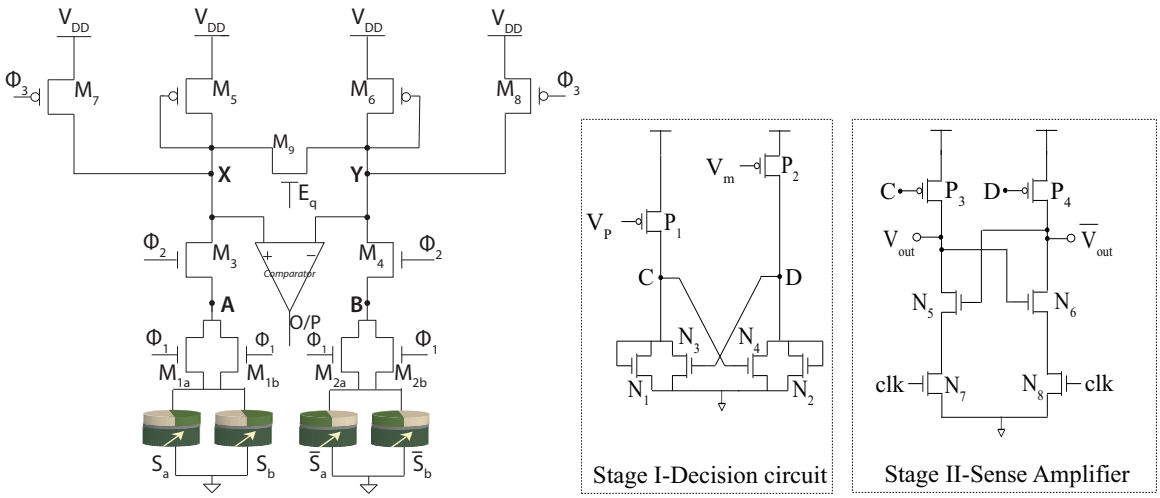


Figure 4.2: Read circuit. (a) Variability tolerant differential read circuit; (b) The two stage comparator [94] with C and D as the points of interconnections. (© 2012 IEEE, with permission.)

Fig. 4.2a shows the read circuit. (M_{1a},M_{1b}) and (M_{2a},M_{2b}) are access transistors of Output cells (S_a, S_b) and their complements ($\neg S_a$, $\neg S_b$). A symmetry is maintained between the transistors in the two arms of the circuit. The access transistors remain on ($\phi_1 = 1$) during the entire read operation. The reading of the cell is carried out in two consecutive phases: Pre-charge followed by Sense.

During the Pre-charge phase, the ϕ_2 signal is pulled low to turn off transistors M_3 and M_4. The active low signal ϕ_3 is pulled down to assist in fast pre-charge of nodes X and Y

to potential V_{DD}. Signal E_q is raised high to equalize nodes X and Y through transistor M_9 so that $V_X = V_Y = V$. During the Sense phase, ϕ_2 is raised to a low voltage, say V_{read}, for applying a low voltage bias on the output MTJs. With $E_q = 0$ and $\phi_3 = 1$, voltage differences start to grow at nodes X and Y due to differential current ΔI through M_5 and M_6 generated by the complementary output states of the MTJs.

Let S_a=S_b=R_0 and $\neg S_a$=$\neg S_b$=R_1, then the currents flowing through X and Y in the sense phase are I_X=nV/R_0 and I_Y=nV/R_1. Here n=2. The larger the differential ΔI=(I_0-I_1)=nV (R_1-R_0)/(R_0R_1), the larger is the sense margin ΔV developed across nodes X and Y. Therefore with increase in n, increase in TMR and decrease in R_1, we can improve the sense margin (see Fig. 4.3). The downside to increasing n is the increase in read power. For example, when R_1=10kΩ and TMR=0.3, the average read power increases from 13.6μW for n=2 to 20.1μW for n=3 and 26.5μW for n=4.

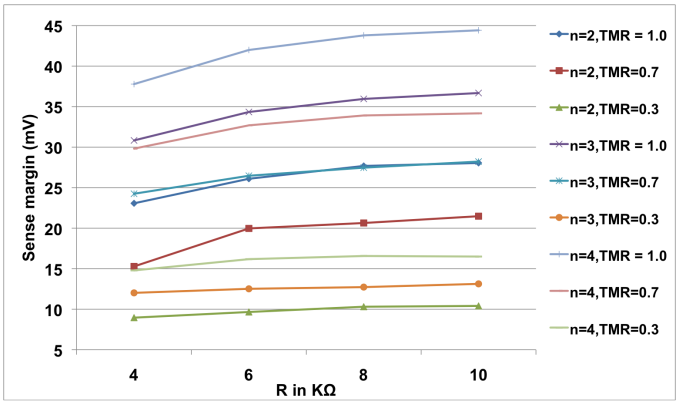


Figure 4.3: Sense margin for different R_1, TMR and n. (© 2012 IEEE, with permission.)

The comparator (Fig. 4.2b) senses the voltage difference and accordingly sets its output V_{out} to either high or low. To summarize the key features of the read circuit:

(i) It is differential with high sense margin and zero cost of reference maintenance;

(ii) It is low power with $I_{read} \ll I_{sw}$;

(iii) It is non-destructive ($I_{read} \ll I_{sw}$) since MTJ states are not flipped during read;

(iv) It is variability tolerant.

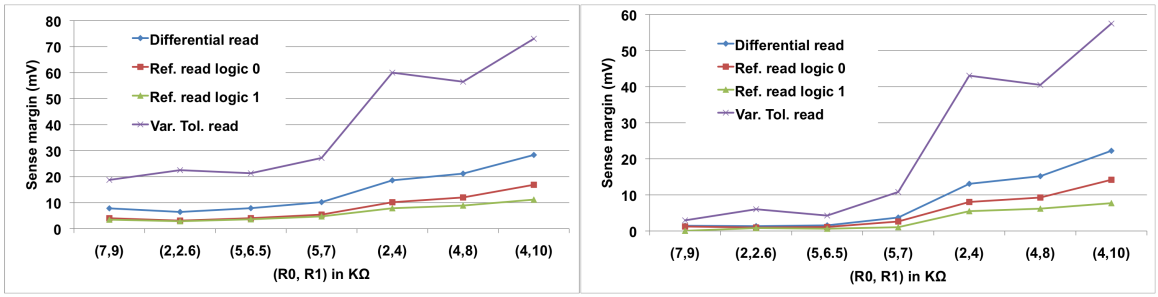
4.5 Analysis of Read Circuit

In this section we have compared the sense margins between reference read, differential read and variability tolerant differential read for different R_0 and R_1. The different read schemes are obtained by differing the resistances on the two arms of Fig. 4.2a. Table. 4.2 compiles the different resistances for the different read schemes. With variations, the sense

Table 4.2: Resistances for different read schemes in Fig. 4.2a.

	Reference Reading	Differential Reading	Variability Tolerant Reading
At A	R_0 or R_1	R_0	(R_0, R_0)
At B	R_{ref} = (R_1+R_0)/2	R_1	(R_1, R_1)

margin gets affected worse when R_0 and R_1 vary in opposite directions so that $\Delta R = R_1 - R_0$ is reduced. With standard deviations of $\sigma_0 = 9.3\%$ and $\sigma_1 = 10.3\%$ [95] in R_0 and R_1, the worst case resistances are $R_0(1+\sigma_0)$ and $R_1(1-\sigma_1)$. Fig. 4.4 shows how the sense margins in the three different read schemes. As expected, the variability tolerant differential read provides the highest sense margin followed by differential read. With worst case variations in MTJ, the sense margin in each read circuit deteriorates as seen in Fig. 4.4b. We can see that even with variations, the sense margin of variability tolerant read circuit remains sufficiently high for reading and is much higher than the other two schemes.



(a) (b)

Figure 4.4: Comparison of reading techniques. Sense margin (mV) in the three different read schemes for different R_0 and R_1 values. Plots are obtained from simulations in 22nm CMOS PTM. Transistor dimensions remain constant across both the plots. (a) Sense margin with no variations; (b) Sense margin with variations. (© 2012 IEEE, with permission.)

4.6 Conclusion

In this chapter we have discussed CMOS aided low power clocking, writing and reading techniques from the architecture. The clock is a stationary equilibrium state achieved with spin transfer torque current. In this chapter we have discussed the theory behind the clock and have derived the clocking current. We have also shown that the clocking current is scalable. The writing technique for the architecture is very similar to memory. Finally we have discussed a variability tolerant differential read technique for the architecture where a pair of outputs are compared against a pair of complements. These CMOS aided operations are on-chip, low power and provide scope for design automation within the architecture.

CHAPTER 5

DEVICE MODELING AND LOW POWER EXTENSIONS

5.1 Motivation

Our STT-MRAM based logic-in-memory architecture uses an integration of magnetic and CMOS planes for computation. To the best of our knowledge we do not have an integrated platform for verifying a magnetic-CMOS co-design. Cadence Virtuoso and OOMMF are standalone suites for CMOS and micromagnetic simulations. Also, micromagnetic simulations are often time consuming. Therefore for fast simulations of the behavior of this architecture and its peripherals we need to have macromagnetic simulation facilities that can be integrated to Cadence Design Environment. We solved this problem through Verilog-A modeling of the multi-layered cells. The model can emulate the behavior of the MTJs in standalone and coupled modes and can be readily instantiated in Cadence Design Environment. Finally we have discussed in this chapter how varying the operating conditions and with different materials we can further reduce the energy consumption of the architecture.

5.2 Elemental Cell Modeling

In this section we will discuss the Verilog-A model of the multi-layered cell. We will first discuss the modeled device parameters followed by the algorithm for modeling.

[0]This chapter was published in parts in IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 1(3): pp. 267-276, 2011, "Low Power Magnetic Quantum Cellular Automata Realization Using Magnetic Multi-Layer Structures", Jayita Das, Syed M Alam, and Sanjukta Bhanja. Permission attached in Appendix A, and
SPIN, World Scientific, 2014, vol. 4(3), " Recent Trends In Spintronics-Based Nanomagnetic Logic", Jayita Das, Syed M Alam, and Sanjukta Bhanja, editor Stuart Parkin. Permission attached in Appendix A.

5.2.1 Device Characteristics Modeling

In order to emulate the theoretical cell behavior in Verilog-A, we have used Eq. 4.11, Eq 4.12 and Eq. 4.16 that describe the critical switching current, the clocking current, and the critical pulse width. We have modeled the resistance dependence of the device as a function of current with the help of Eq. 4.19 and Eq. 4.20. The intrinsic device parameters used in the model are kept consistent with the values available in literature and are outlined in Table 5.1.

Table 5.1: Device parameters used in simulation.

Device Parameter	Values
Dimension (L×W×d)	$100\times50\times2nm^3$
Ref. Layer coupling field, H_d	2500A/m
Damping constant, α	0.01
Saturation Magnetization, M_s	$8e5$A/m
Spin-polarizing factor, P	0.4
Anisotropy field, H_k	10Oe

5.2.2 Neighbor Interaction Modeling

We have employed a Finite State Machine to model the cell behavior under the influence of its neighbors. To personate the cell behavior, we have developed two models of multi-layer cells - the horizontal cell and the vertical cell (see Fig. 5.1). We recommend the horizontal cell for horizontal interconnects and the vertical cell for vertical interconnects. The cell behaviors are however identical in a majority logic configuration with three inputs.

Fig. 5.1a shows a horizontal cell H with three inputs T, B and L. The output from H acts as input to the cell R on its right. We have modeled the cell with two electrical inout ports that can be used for CMOS integration. The two ports also takes into account the electrical resistance of the device. To model the magnetic behavior, we have modeled each cell with four magnetic ports, one on each side. The magnetic ports $\mathbf{m_T}$, $\mathbf{m_L}$, $\mathbf{m_B}$, and $\mathbf{m_R}$ are virtual bi-directional dual ports that we have designed to collect information about

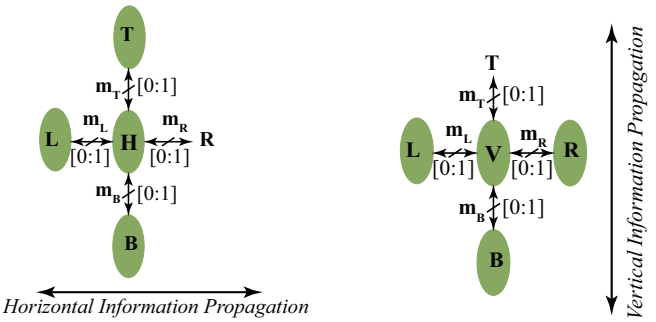


Figure 5.1: Modeling neighbor interaction. (a) A horizontal cell H; (b) a vertical cell V. T, L, B and R represents the neighbors on the top, left, bottom and right of H and V. $\mathbf{m_T}$, $\mathbf{m_L}$, $\mathbf{m_B}$ and $\mathbf{m_R}$ are virtual dual bi-directional magnetic ports that helps to communicate the state of a cell with that of its neighbor. (© 2011 IEEE, with permission.)

the state of neighbors on the top, left, bottom and right. The bidirectional ports are also used to communicate that state of the cell to its immediate neighbor. The port details are compiled in Table 5.2. The state of H is then computed with the help of a Finite State Machine and the states of the inputs T, L and B. This also ensures that information only flows from the inputs to the output and not in the opposite direction. The model currently uses the magnetostatic interaction from only the immediate neighbors to the top, bottom, and left to determine the state of H. Contentions in the case of two inputs are resolved in the model by giving one coupling priority over the other. We have used 2 bits to represent the three different states of a cell: 11 for Logic 1, 00 for Logic 0 and 01 for Clocked. Fig. 5.1b shows a vertical cell V with neighbors on its left, right and bottom. The cell is modeled similar to the horizontal cell. The FSM for the horizontal and the vertical cell are described in Algorithm 2 and Algorithm 3. The FSM represents the post-clocking behavior of H and V.

The model is generic. It can simulate the behavior of a cell with 1-3 inputs. For n $<$ 3 inputs, the relevant magnetic port of the cell facing the input is pinned to 01. To simulate a horizontal wire, the ports $\mathbf{m_T}$ and $\mathbf{m_B}$ of every cell except the input are to be connected to 01. To simulate a vertical wire, the ports $\mathbf{m_L}$ and $\mathbf{m_R}$ of every cell except the input are to be connected to 01. The Verilog-A model of the multi-layer device has been simulated

Table 5.2: Ports of the multi-layered cell model.

Ports	Type	Direction	Function
$\mathbf{r_f}$	Electrical	Inout	Free Layer
$\mathbf{r_p}$	Electrical	Inout	Fixed Layer
$\mathbf{m_A}$	Magnetic	Bi-directional	coupling with left
$\mathbf{m_B}$	Magnetic	Bi-directional	coupling with right
$\mathbf{m_C}$	Magnetic	Bi-directional	coupling with bottom
$\mathbf{m_D}$	Magnetic	Bi-directional	coupling with top

using Cadence Spectre for device dimensions of $100 \times 50 \times 2\text{nm}^3$. The device model has been integrated with 22nm predictive CMOS technology [96] and the spin-transfer torque switching has been verified.

```
if A = B = C = clocked  then
  V = U
else if A = B = clocked then
  V = C
else if A = C = clocked then
  V = B
else if A = clocked then
  if B=C then
    V=B.C
  else
    V=U
  end if
else if B = C = clocked then
  V = ¬ A
else if B = clocked then
  V = C
else if C = clocked then
  V = B
else
  V = B . C + ¬A . (B ⊕ C)
end if
```

Algorithm 2: Horizontal cell. (© 2011 IEEE, with permission.)

```
if A = B = C = clocked  then
  H = U
else if A = B = clocked then
  H = C
else if A = C = clocked then
  H = ¬B
else if A = clocked then
  H = C
else if B = C = clocked then
  H = ¬A
else if B = clocked then
  H = C
else if C = clocked then
  if A = B then
    H =¬A
  else
    H = U
  end if
else
  H = C . ¬B + ¬A. (¬B + C)
end if
```

Algorithm 3: Vertical cell. (© 2011 IEEE, with permission.)

5.3 Low Energy Extensions of the Architecture and CMOS Comparison

Advantages of the logic-in-memory architecture over CMOS includes: (i) non-volatility; (ii) less area [97]; (iii) scope of reconfigurability (with the basic AND/OR logic sharing the same footprint with majority); (iv) thermal robustness; and (v) radiation hardness. For example, high temperature affects the circuit speed in CMOS [98], and at $65nm$ CMOS technology node there is a delay variation of as high as 51.6% in a 2-input NAND operating at a nominal supply voltage of 1V. Thermal robustness of the MTJs would enable the architecture to operate beyond the operating range of temperature for CMOS.

In this section we have explored four possible ways in which we can further reduce the switching energy of the architecture to make it comparable to modern CMOS [80]. The techniques include: (i) Supply voltage scaling; (ii) Operation in adiabatic regime; (iii) Use of

multiferroics [97, 99]; and (iv) Use of perpendicular MTJs or p-MTJs [100]. Below we have discussed each of the techniques and provided a comparative study with CMOS.

(i) Supply voltage scaling: For $R_1 = 2.6K\Omega$ and $R_0 = 2K\Omega$, a potential of 650mV and 442mV should be sufficient to provide the required clocking and writing current. Since clocking activity dominates over writing in a logic, scaling down the supply to half can cut down the energy consumption by one fourth. However, the sacrifice on timing is less since the device still operates in the precessional switching range [16].

(ii) Operation in the adiabatic regime: Operating the logic in the adiabatic regime, will result in energy dissipation equivalent to the energy barrier of the individual MTJs [101]. In Section 2.3.3, we have seen that the energy barrier generated out of the shape and uniaxial anisotropy in inplane nanomagnetic structures of dimensions $100 \times 50 \times 2$ nm^3 is $\approx 1200k_BT \approx 4.9aJ$. With reasonable accuracy we can approximate this to the energy barrier of the free layer of a MTJ with similar dimensions. Therefore, a substantial reduction in switching energy can be achieved by operating the logic in the adiabatic region (see Table 5.3). However, the trade-off is in speed (by an order of one or two) [51].

(iii) Use of multiferroics: This is a material engineering approach. Using multiferroic cells [97, 99] can reduce clocking energy to as low as 0.2fJ per cell with a clocking speed as high as 2.5GHz. These values are comparable to modern CMOS. This is an active research area and one of its present challenges is its CMOS integration.

(iv) Use of p-MTJs: Use of p-MTJs can reduce the switching current to as low as $9 \pm 2kA/cm^2$ [100] with the same order of computational speed as inplane NML [102]. For our MTJ dimensions this would equal a switching current of $\approx 0.5\mu A$. Given that the switching and the clocking currents are roughly of the same order, p-MTJs can reduce

the switching energy consumption by as much as 500^2 times, assuming same MTJ resistance and switching time as the inplane ones used in the architecture.

Table 5.3 compiles the results of switching energy for a fanout of 4 (FO4) inverter and a 2-input NAND from the different techniques and CMOS (high performance HP and low power LP) [97]. Table 5.4 presents a comparison of leakage power for a 2-input AND at 135°C between different techniques and 22nm CMOS. The CMOS simulations are carried out in HSPICE using 22nm PTM.

Table 5.3: Switching energy consumptions in fJ. (© 2014 SPIN, with permission.)

Circuit	STT-NML	Supply scaling	Adiabatic	Multiferroics	p-MTJ	CMOS HP	CMOS LP
Inv FO4	0.65e3	0.292e3	9.8e-3	0.4	2.6e-3	≈ 0.1	≈ 0.01
2-input NAND	1.3e3	0.585e3	18.6e-3	0.8	5.2e-3	≈ 0.1	≈ 0.01

Table 5.4: Leakage power consumption at 135°C. (© 2014 SPIN, with permission.)

Circuit	STT-NML	Supply scaling	Adiabatic	Multiferroics	p-MTJ	22nm CMOS PTM
2-input AND	0	0	0	0	0	$\approx$ 2.5nW (at V_{DD}=1V)
2-input OR	0	0	0	0	0	$\approx$ 1.6nW (at V_{DD}=1V)

5.4 Conclusion

In this chapter we have described a macromagnetic model of the MTJs in Verilog-A. The model can be integrated into Cadence Design Suite for CMOS-magnetic co-simulation of the architecture behavior. We have modeled two types of cells: horizontal and vertical for the two orthogonal directions of information propagation. The cells are designed with two bidirectional electrical ports and four bidirectional magnetic ports to interact with the neighbors. We have used finite state machines to determine the output of each type of cell. In this chapter we have also discussed how material engineering and careful selection of operation condition can significantly reduce the switching or dynamic energy of the architecture to the range of modern CMOS. We have also shown a comparison of the leakage between the architecture and advanced CMOS both operating at high temperatures.

CHAPTER 6

SOLUTIONS TO HIGH DENSITY LOGIC

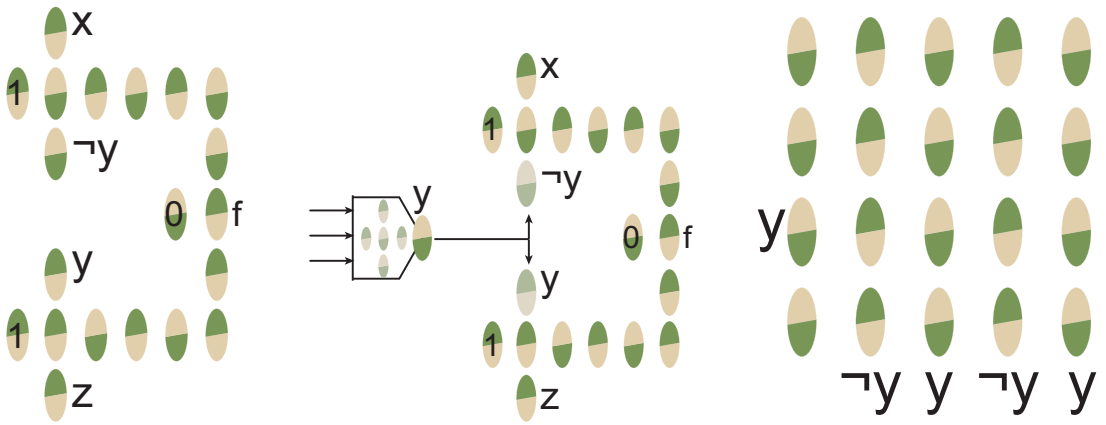
6.1 Motivation

Let us consider a AND-OR synthesized logic function $f(x, y, z) = (x \wedge \neg y) \vee (y \wedge z)$ (see Fig. 6.1a). Now consider the case where y is not a primary input but an output of a gate from a previous stage. With a regular cell layout that we have in our architecture or to be more generic in nanomagnetic logic we can either get y or $\neg y$ in a column (see Fig. 6.1b). This is because information only proceeds in a row through antiferromagnetic coupling, which requires adjacent cells to have complementary values (see Fig. 6.1c). We define this as the layout constraint problem. The popular technique to increase throughput is to pipeline the logic operations. Again in field-coupled logic it is the nature of clock independent of its implementation that generates a conflict between pipelined operation and high-density logic layout. We define this as the high-density pipeline problem. In this chapter we have discussed these two problems and their possible solutions.

6.2 Layout Constraint Problem

Let us look into the logic function $f(x, y, z) = (x \wedge \neg y) \vee (y \wedge z)$, where y is the output of a gate. Say $y = f(x_1, \ldots, x_n)$. With the layout constraint a regular layout cannot generate y and $\neg y$ on the same column. One solution to the problem is to apply De Morgan's Law to

[0]This chapter was published in parts in 12th IEEE Conference on Nanotechnology (IEEE-NANO), pp 14, 2012, " Addressing The Layout Constraint Problem When Cascading Logic Gates In Nanomagnetic Logic", Jayita Das, Syed M Alam, and Sanjukta Bhanja. Permission attached in Appendix A. and
14th IEEE Conference on Nanotechnology (IEEE-NANO), 2014, " Prospects For Pipeline in High-Density Magnetic Field-Coupled Logic", Jayita Das, Syed M Alam, and Sanjukta Bhanja.



(a) (b) (c)

Figure 6.1: Explaining layout constraint. Implementation of $f(x, y, z) = (x \wedge \neg y) \vee (y \wedge z)$ with (a) x, y and z as primary inputs; (b) y as output from previous stage of logic; (c) regular layout and origin of layout constraint.

generate $\neg y$ from primary inputs. However, this solution is both costly in area and power. The problem becomes more significant when we have cascaded logic. We can understand it with the help of the two propositions P_1 and P_2 from De-Morgan's Law, where

$$\neg(P_1 \wedge P_2) \Leftrightarrow (\neg P_1) \vee (\neg P_2) \tag{6.1}$$

$$\neg(P_1 \vee P_2) \Leftrightarrow (\neg P_1) \wedge (\neg P_2) \tag{6.2}$$

Which means if y can be represented as $y = P_1 \wedge P_2 \wedge P_3 \wedge \ldots P_n$, then $\neg y$ can be represented as $(\neg P_1) \vee (\neg P_2) \vee (\neg P_3) \vee \ldots \vee (\neg P_n)$. Now if $P_i|_{i \in 1,\ldots,n} = x_1 \vee x_2 \vee \ldots \vee x_j$, where $x_1, \ldots x_j$ are the primary inputs of the logic then $\neg P_i = (\neg x_1) \vee (\neg x_2) \vee \ldots \vee (\neg x_j)$. If the complementary of the primary inputs are readily available or generated through antiferromagnetic coupling, then P_i and $\neg P_i$ have the same footprint. This comes from the reconfigurability between AND and OR in field-coupled magnetic logic (Section 2.3.2). Therefore using De Morgan's rule $\neg y$ can be generated in the same column as y but the solution is not satisfactory in terms of area and power.

6.3 Classical Example

A classical example of the layout constraint problem is the n-input XOR, where n≥ 3. Since, XOR is an important component in any datapath circuit, the problem is of critical importance. So solving this problem would help to reduce the overall area and power consumption from arithmetic and logic circuits. Here we will consider the 3-input XOR, which is also the sum output of a full adder. Its logic function is given by:

$$f(x_1, x_2, x_3) = (x_1 \wedge \neg x_2 \wedge \neg x_3) \vee (\neg x_1 \wedge x_2 \wedge \neg x_3) \vee (\neg x_1 \wedge \neg x_2 \wedge x_3) \vee (x_1 \wedge x_2 \wedge x_3) \quad (6.3)$$

where x_1, x_2 and x_3 are the primary inputs. The implementation in this form would take four 3-input AND and one 4-input OR, which boils down to eight 2-input AND gates and three 2-input OR gates. If the footprint of a 2-input AND/OR is x, this particular function implementation would occupy a total area of $11x$. Eq. 6.4 and Eq. 6.5 give a more economic implementation of the function through grouping and reuse.

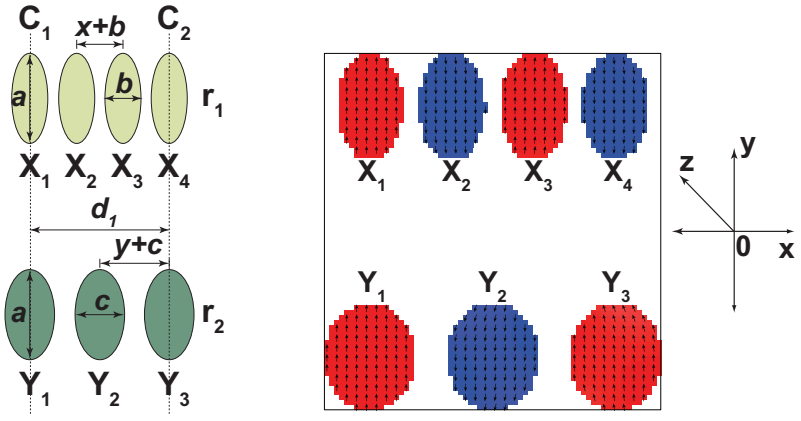
$$f(x_1, x_2, x_3) = (x_1 \oplus x_2) \oplus x_3 = (y \wedge \neg x_3) \vee (\neg y \wedge x_3) \quad (6.4)$$

where

$$y = x_1 \oplus x_2 = (x_1 \wedge \neg x_2) \vee (\neg x_1 \wedge x_2) \quad (6.5)$$

y requires two 2-input AND and a 2-input OR. By substituting y for $x_1 \oplus x_2$, we can reduce the total gate count to four 2-input AND, two 2-input OR and one NOT, provided we figure out a way to generate y and $\neg y$ in the same column. A NOT gate in field-coupled magnetic logic occupies half the area of a 2-input AND/OR gate. Therefore the total footprint of the logic reduces to 6x+0.5x=6.5x. This is a reduction of more than 40%. This also translates to a reduction in power, since each cell in the logic is either clocked or written. This

calculation neglects the power and area consumption in the interconnects, which will also scale in proportion to the number of gates in the logic.



(a) (b)

Figure 6.2: Solution to layout constraint problem. (a) Geometrical placement of cells for solution to layout constraint. The design parameters are listed in Table 6.1; (b) OOMMF simulation output of clocking of the two horizontal rows r_1 and r_2. The cell labels are consistent with Fig. 6.2a. Red and blue indicates magnetization in opposite directions. (© 2012 IEEE, with permission.)

6.4 Novel Solution to the Problem

Here we have proposed two possible solutions to the layout constraint problem [103].

(i) Solution 1: Read out and write back.

(ii) Solution 2: Introduce irregularity.

Solution 1 would require reading out the outputs, complementing it and then writing it back in its complemented form. However, in this chapter we would focus on the second solution. Fig. 6.2a shows the two rows of interconnects that are used for Solution 2. Depending on the number of cells used in the rows, the cell dimensions and their spacing in the two rows will vary. The dimensions and spacing should be suitable for effective room temperature operations. We have chosen a 4:3 ratio of cells. The dimensions of $X_1, \cdots, X_4$ and $Y_1, \cdots, Y_3$ and their spacing in rows r_1 and r_2 should be able to vertically align the two rows at C_1 and

C_2. At the same time the spacing should be sufficient to provide effective inter cell dipolar coupling. Fig. 6.2b presents the post clocked simulated outputs of the two rows of cells. For confirming the validity of solution we have simulated single layer permalloy cells in OOMMF simulator [50]. All the design and simulation parameters are tabulated in Table 6.1. A and K_1 are the exchange coefficient and crystalline anisotropy constant of permalloy.

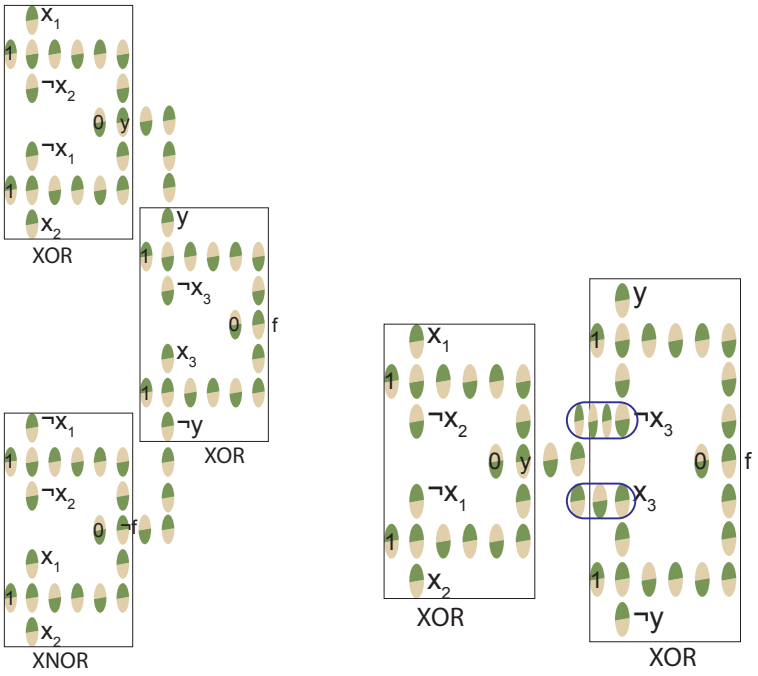
Table 6.1: Parameters used for solution.(© 2012 IEEE, with permission.)

Design and Simulation parameters.		
a=100nm	b= 40nm	c= 55nm
x= 11.33nm	y=22nm	d_1 = 154nm
Material = Permalloy		Cell size = $5 \times 5 \times 5$
$K_1 = 100 J/m^3$		A = 13*e*-12J/m

The simulations show successful information propagation along the right. The two rows of cells are separated far enough to prevent any interactions between the rows. For the simulation, X_1 and Y_1 were marked as the input cells and their magnetizations are fixed along the +y direction for the entire simulation. The initial magnetization of the rest of the cells were aligned along the +x direction to replicate the clocked state of the cells. The cells were then left to precess with the start of the simulation. The final settlement of all the cells is observed in Fig. 6.2b and is in complete agreement to the states of the inputs. Fig. 6.3b shows the 3-input XOR with the proposed solution. It is comprised of two 2-input XORs cascaded together as described by the logic function. Here the interconnects resolve the layout constraint and are encircled in green. With this solution, the reduction in cell count and power for a 3, 4 and 5-input XOR are shown in Fig. 6.4a and Fig. 6.4b.

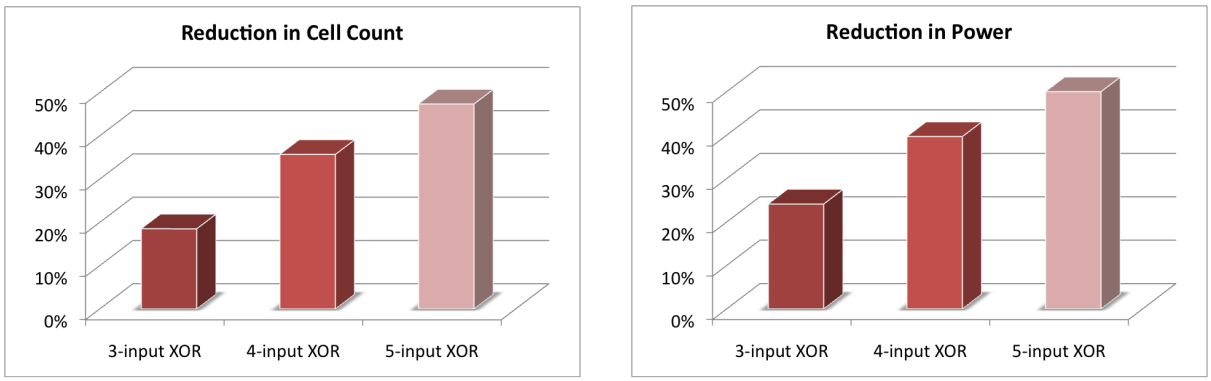
6.5 High-Density Pipeline Problem

For a better understanding of the problem let us look into the clock propagation within logic. The function of clock is to destabilize the cells in order to aid computation. Overhead and underneath metal lines running parallel to rows are used to carry the clock current.



(a) (b)

Figure 6.3: 3-input XOR. (a) Traditional layout; (b) with the proposed solution.



(a) (b)

Figure 6.4: Improvement with introduction of selected irregularities. Percentage reduction in (a) cell count with the solution; (b) power with the solution. (© 2012 IEEE, with permission.)

During logic computation, the states φ_i of cells fall into one of the three categories [104], i.e. $\varphi_i \in$ {HOLD (H), RESET (R), SWITCH (S)} (see Fig. 6.5a). R is the clocked state and S & H are the non-clocked states for the cells. Also, for unidirectional flow of information through the logic, a Δ overlap is needed between the adjacent phases $(\phi_j, \phi_{j+1})|_{j=\{0,1,\cdots,n-1\}}$

of clock [104]. This would ensure that when a cell is in S state, the cells in its next clock zone (towards the outputs) are in R state and do not influence its ground state and the cells in its previous clock zone (towards the inputs) are in H state and decides its ground state.

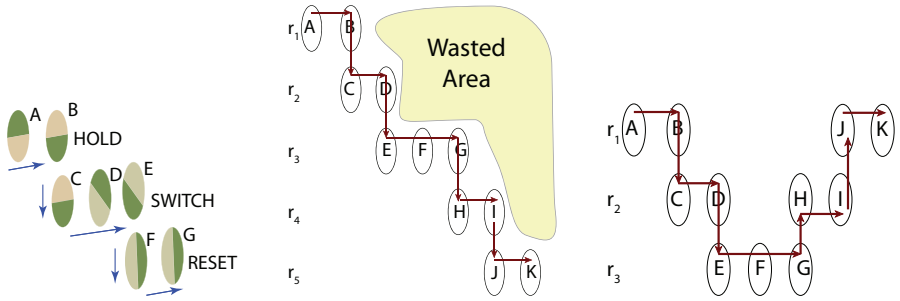


Figure 6.5: Logic states and staircase information propagation. (a) Logic states $\varphi_i \in$ {H,S,R}. H: cells with definite logic value; S: cells relaxing towards their ground state upon clock release; R: clocked cells. The arrows indicate the direction of information flow. (b) A layout of cells where information flows from A to K. Arrows indicate the direction of information flow. Note the wasted area from the staircase fashion of information flow. (c) A more area efficient layout of cells where information flows from A to K. It saves an area equivalent to 2 rows. (© 2014 IEEE, with permission.)

Fig. 6.5 shows two instances of information flow. Fig. 6.5c is the preferred choice of cell layout since it saves area equal to two rows. However, in Fig. 6.5c information in the left arm A to E and in the right arm G to K need to flow in opposite directions. This is a problem if an entire row of cells is clocked at the same time. In the next section we will discuss this problem in greater details. The situation becomes further complicated when the logic is operated in pipeline [104]. Though previous works have addressed the concept of n-phase clock and pipeline [104, 52], none have addressed the problem of high density and pipeline at the layout level. In this chapter we have shown possible solutions to the problem with the help of CMOS control, an additional cell state and a slower clock [105].

6.6 Mathematical Description

In Fig. 6.5c the information flow from D to H can be partitioned into steps D to E, E to G and G to H. From the conditions of clocking mentioned in the previous section and

described by Fig. 6.5a, when E, F, G are switching or in S state C, D needs to be in H state and H, I needs to be in R state. This means that cells (D, E) and (H, I), which share the same row r_2 need to be in two different states φ_i at the same time. One of them needing and the other not needing a clocking current.

Given that we require minimum of three cell states to propagate information (see Fig. 6.5a) and if the average time that a cell spends in any one state is T then the minimum clock period T_{clkmin} = 3T. In Fig. 6.6 we have shown a 3-phase clock propagation through the layout of Fig. 6.5c. The current scenario is non-pipelined. For two adjacent rows r_i and r_{i+1} that are clocked in phases $\phi_j|_{j=\{1,2,3\}}$ and $\phi_{j'}|_{j'=\{1,2,3\}}$ and j≠j', the relation $\phi_{j'}(t) = \phi_j(t+T)$ should hold for information to flow from $r_i \rightarrow r_{i+1}$. This is because the cells in r_i need to be in H state when cells in r_{i+1} are in S state for information to flow from $r_i \rightarrow r_{i+1}$. Similarly, for information to flow in the reverse direction from $r_{i+1} \rightarrow r_i$ the relation $\phi_j(t) = \phi_{j'}(t + T)$ should hold. Therefore, for information to flow from $r_i \rightarrow r_{i+1} \rightarrow r_i$ the relation $\phi_j(t) = \phi_j(t+2T)$ should hold, which implies T_{clk} = 2T should hold, which is in violation to T_{clkmin}=3T. The situation becomes even more complex when the system operates in pipeline. We have discussed this in Section 6.7 and Section 6.8.

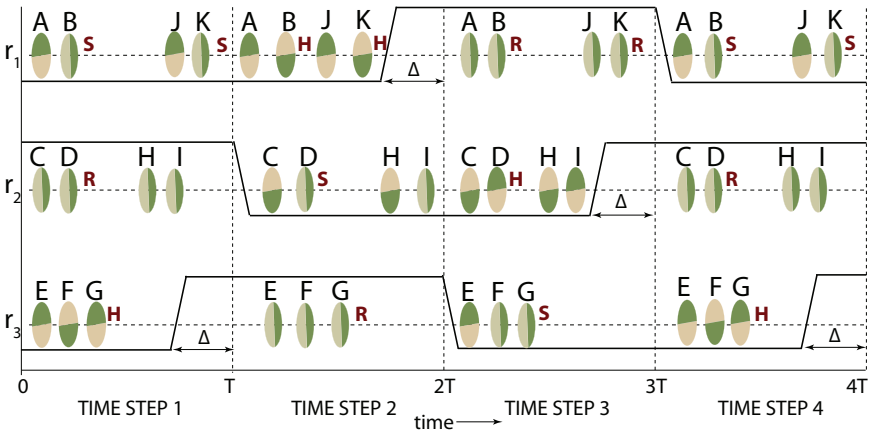


Figure 6.6: 3-phase clock propagation. The layout is of Fig. 6.5c. The cell states φ_is are mentioned alongside in red. (© 2014 IEEE, with permission.)

6.7 3-phase Clock

In a n=3-phase clock, the cell states follow this order R→S→H (see Fig. 6.6) A cell is first clocked. It is then released when it switches and settles for a ground state. Finally, it holds onto its state to serve as input to the next cell. The clock time period is T_{clk}=3T. Table 6.2 outlines three consecutive time steps and the corresponding cell states in the non-pipelined logic shown in Fig. 6.6. We see that in every time step, the state φ_i of (C, D) in the left arm of row r_2 and the state φ_j of (H, I) in the right arm of r_2 are different, i.e. i≠j. Let's analyze it further. In time steps t_0+T, φ_i=S and φ_j=H. These are both unclocked states. In time steps t_0+2T and t_0+3T, however one arm requires clocking while the other arm does not.

Table 6.2: Cell states in three consecutive time steps of 3-phase clock. (© 2014 IEEE, with permission.)

	Cell states							
	Non-pipelined operation			Pipelined operation				
Time	(C, D)	(E, F, G)	(H, I)	(A, B)	(C, D)	(E, F, G)	(H, I)	(J, K)
t_0+T	S	R	H	H	S	R	H	R
t_0+2T	H	S	R	R	H	S	R	S
t_0+3T	R	H	S	S	R	H	S	H

These conflicting requirements on the cell states of r_2 in time steps $t_0 + 2T$ and $t_0 + 3T$ can be resolved if the cells in r_2 are equipped with access transistors. These transistors can be used to cut off the clock current supply from the desired cells while the remaining cells in the row remain clocked. Therefore, by turning off the access transistors in the left arm of r_2 during t_0+2T and turning off the transistors in the right arm of r_2 during t_0+3T we can send information from D to H via E, F, G. However, the metal pitch of 22nm CMOS would only allow one access transistor for every alternate cells in a row (Section 3.5). Therefore, all the cells in r_2 cannot have access transistors. Let us further look into the nature of information flow in Fig. 6.5c to pick up cells that need to have access transistors for correct information propagation. Note, information has to flow by D to reach E from C. Therefore D should have

an access transistor. Similarly information needs to flow by H to reach I from G. Therefore H should have an access transistor.

With pipeline, once the pipeline gets full every row will actively participate in information flow in every time step. Table 6.2 outlines the required cell states in the three rows of Fig. 6.5c for correct information propagation. Let us look into row r_1. In time steps t_0+T and t_0+2T, the cells in the left and right arm of r_1 are simultaneously in clocked and unlocked state. But as we discussed in Section 3.5, we can have only one access transistor for every 2×2 cells. This means only alternate rows can have access transistors. Since row r_2 has access transistors, r_1 cannot have access transistors. Therefore, with 3-phase clock we cannot obtain pipelined operation on high-density logic layout. Pipelined logic with 3-phase clock can only work if the layout is in staircase fashion (see Fig. 6.5b). In the next section we will see how we have solved this problem by introducing an additional state in the cells and increasing the clock period.

6.8 4-Phase Clock

Fig. 6.7 shows a 4-phase clock propagation through any logic. We have introduced an additional I or IDLE state in the cells. This is the state when a cell does not actively participate in logic computation or its state is not important to the logic computation. Table 6.3 compiles the states of the cells from four consecutive time steps of clock propagation on Fig. 6.5c when the logic operates in non-pipelined mode.

From Table 6.3 we once again see that the two arms of r_2 needs to be in clocked and unclocked state in the same time steps $t_0 + 2T$ and $t_0 + 4T$. As we have discussed in the previous section, we can solve this problem with the help of access transistors with cells D and H. For non-pipelined operation, 4-phase clock would also not incur any additional delay for the information to flow from A to K.

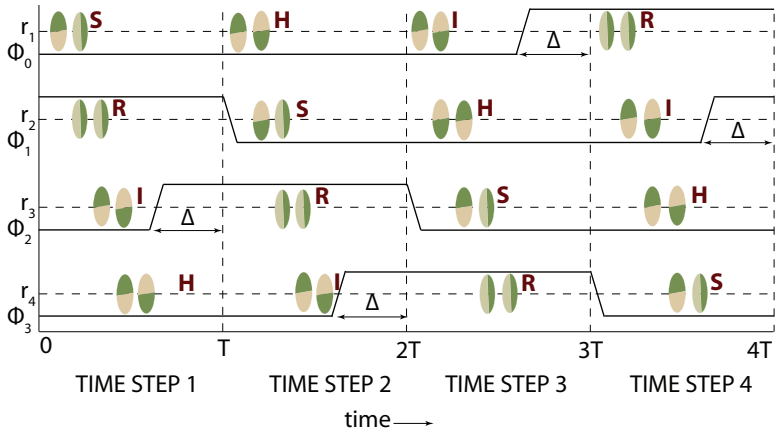


Figure 6.7: 4-phase clock propagation. r_1, r_2, r_3 and r_4 are consecutive logic rows. In addition to R, S and H states, the cells now have an IDLE (I) state. (© 2014 IEEE, with permission.)

Table 6.3: Cell states in four consecutive time steps with 4-phase clock. Layout is that of Fig. 6.5c. (© 2014 IEEE, with permission.)

	Cell states							
	Non-pipelined operation			Pipelined operation				
Time	(C, D)	(E, F, G)	(H, I)	(A, B)	(C, D)	(E, F, G)	(H, I)	(J, K)
t_0+T	S	R	I	H	S	R	I	H
$t_0 + 2T$	H	S	R	I	H	S	R	I
$t_0 + 3T$	I	H	S	R	I	H	S	R
$t_0 + 4T$	R	I	H	S	R	I	H	S

Table 6.3 compiles the cells states under pipelined operation for the layout in Fig. 6.5c. We can now see that the left (A,B) and right (J,K) arms of r_1 are always in the same state even though they are propagating information in opposite directions. This has become possible with the addition of the I cell state. Therefore, with 4-phase clock we can now realize pipelined operation together with layout flexibility. The tradeoff is the delay of one phase duration T. Assuming every row is clocked in a single phase of clock, and there are N such rows (counting a row twice if it carries information in opposite directions) in a m-bit output logic, the delay and throughput from 3 and 4-phase clock are outlined in Table 6.4.

Table 6.4: Delay and throughput from multiphase clock. Logic operations in both non-pipelined and pipelined mode over flexible high-density layouts. (© 2014 IEEE, with permission.)

	Non-pipelined operation		Pipelined Operation	
n-phase	Delay	Throughput	Delay	Throughput
3	(2+N)T	m bits/(2+N)T	-	-
4	(3+N)T	m bits/(3+N)T	(3+N)T	m bits/T

6.9 Conclusion

In this chapter we have addressed a layout constraint problem which poses a severe challenge to cascading. After describing the origin of the problem, we have presented a solution that involves introducing localized irregularities in the layout. We have also discussed a clock propagation problem and tradeoffs with flexible high density logic layouts. If information flows along $r_i \rightarrow r_{i+1} \rightarrow r_i$ in non-pipelined fashion, access transistors need to be placed underneath cells in row r_i that are at the intersection with r_{i+1}. Thereafter, we have shown that for pipelined operation, a 3-phase clock is not sufficient together with flexibility of layout and saving of area. We need a 4-phase clock with an additional I state in cells.

CHAPTER 7

LOGIC PARTITIONING

7.1 Introduction

In this chapter we have focused on enhancing the performance of datapath elements in the architecture. As we have seen the architecture is an integration of magnetic and CMOS planes. The computation takes place in the magnetic plane while the ordering and control takes place from the CMOS plane. In this chapter we have taken the help of Shannon expansion of logic to re-adjust the share of responsibilities between the two planes to achieve an overall improvement in (i) cell count; (ii) energy; and (iii) delay for datapath elements. Here we have studied the methodology over 2-input and 3-input XOR that are the basic elements of datapath circuits [106, 107]. By this new re-distribution technique we have increased the overhead on CMOS peripherals in certain operating periods. However, with the tremendous savings in cell count that we achieved, such overhead periods have been limited and an overall savings in the power consumption in CMOS is achieved as well.

7.2 Traditional XOR Design

In Section 3.9 we have already studied the layout of a 2-input XOR in the architecture. For convenience we have reproduced it in Fig. 7.1a. It consists of three logic blocks and

[0]This chapter was published in parts in 12th IEEE Conference on Nanotechnology (IEEE-NANO), pp 1-6, 2012, " A Novel Design Concept For High Density Hybrid CMOS- Nanomagnetic Circuits", Jayita Das, Syed M Alam, and Sanjukta Bhanja. Permission attached in Appendix A, and
IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 22(1), pp. 90-98, 2014 " Nano Magnetic STT-Logic Partitioning for Optimum Performance", Jayita Das, Syed M Alam, and Sanjukta Bhanja. Permission attached in Appendix A.

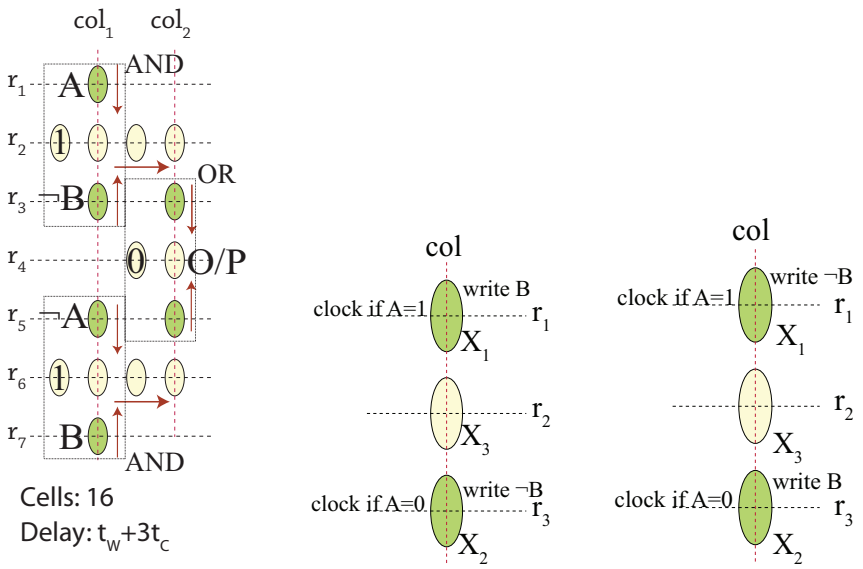


Figure 7.1: 2-input XOR. (a) Traditional design. Arrows indicate direction of logic flow; (b) New design; (c) New 2-input XNOR. (© 2014 IEEE, with permission.)

two interconnect segments. M_1 and M_2 performs A∧¬B and ¬A∧B. M_3 performs $M_1 \vee M_2$, which is the desired result. The operation sequence for the logic is detailed in Algorithm 1. The cell count for the logic is 16. The total delay is $t_w + 3t_{clk}$, where t_w and t_{clk} are the write and clock durations.

7.3 Theory Behind New Design

From the well-known Shannon's expansion theorem, a logic function of n variables x_1, x_2, ..., x_i, ..., x_n, can be factored into a single variable x_i and its cofactor f_i [108] as shown in Eq. 7.1.

$$f(x_1, x_2, \ldots, x_i, \ldots, x_n) = (x_i \wedge f_i(x_1, x_2, \ldots, 1, \ldots, x_n)) \vee (\neg x_i \wedge f_i(x_1, x_2, \ldots, 0, \ldots, x_n)) \tag{7.1}$$

In our new design, we have singled out variables at different stages of logic followed by assigning the responsibilities of the singled out variable to the metal lines and CMOS peripherals. The execution responsibility of the cofactor is left with the magnetic plane. For a

2-input XOR the logic function f(A,B)=(A∧¬B)∨(¬A∧B) is already in the expanded form of Eq. 7.1. If we single out variable A, then the output should be either ¬B or B depending on A=1 or A=0. In our approach, the variable A that is singled out is not written explicitly into any Input cell. Rather the operations corresponding to its appropriate cofactor, here ¬B or B, are carried out in the MTJs. The controls for the cofactor execution are sent through the metal lines depending on the value of the singled out variable. In the next few sections we have described the operation sequence for 2-input XOR, 3-input XOR and the majority.

7.3.1 2-input XOR

The new design for the 2-input XOR requires a total of 3 cells X_1, X_2 and X_3 (see Fig. 7.1b). A and B are the inputs. Both X_1 and X_2 are Input cells. Algorithm 4 outlines the operating sequence for the logic. Fig. 7.2 shows the cell states during the different phases of operation.

Input: A, B.
Output: X_3= A⊕B.
Logic sequence:
Phase I : Write $X_1 = B$ and $X_2 = \neg B$
Phase II : Clock X_3
if A = 1 **then**
  Clock X_1
else
  Clock X_2
end if
Phase III: Release the clock for X_3.
Phase IV : Deactivate all metal lines.

Algorithm 4: New 2-input XOR. (© 2014 IEEE, with permission.)

In the first phase the value of the two cofactors are written into the two Input cells. In the second phase, X_3 is clocked along with X_1 or X_2 depending on the value of A. Clocking of either X_1 or X_2 with X_3 ensures that the final output in X_3 is influenced only by the desired input X_2 or X_1. In the third phase the clock for X_3 is released so that it can orient according

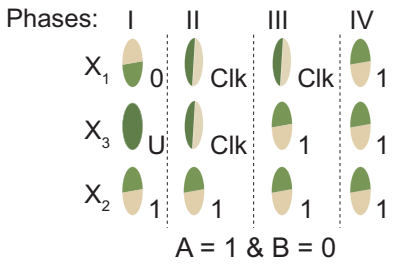


Figure 7.2: The top view of cells for A=1 and B=0 during different phases. U is a don't care state. (© 2014 IEEE, with permission.)

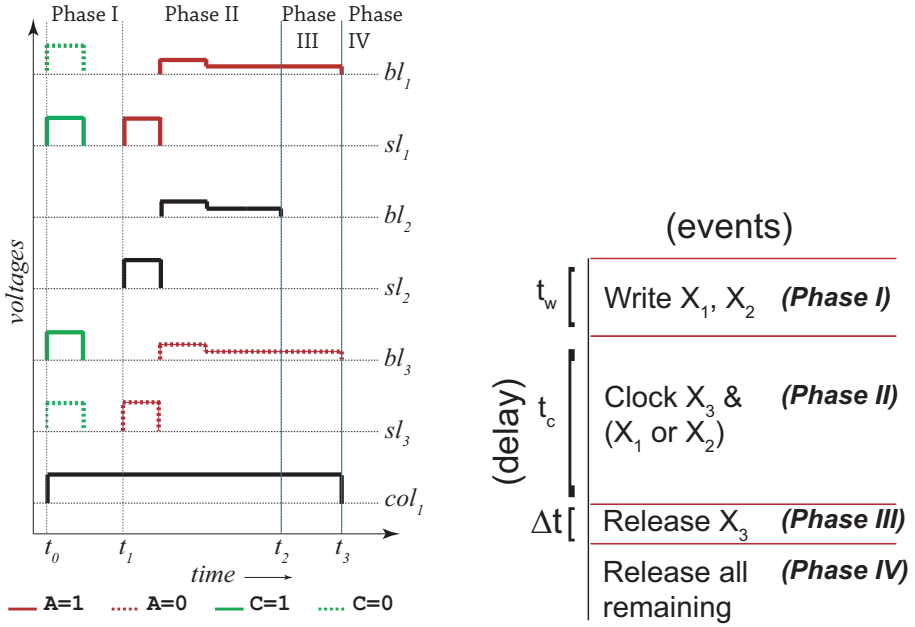


Figure 7.3: Voltage signals and delays. (a) The voltages at the bit (BL), source (SL) and wordlines (col) during different phases. The subscripts in BL and SL denote the corresponding row numbers. t_w = t_1 - t_0, t_c=t_2-t_1 and Δt=t_3-t_2. $\Delta t \ll t_c$. (b) Delay of different phases of the novel 2-input XOR. (Voltage signals not drawn to scale.) (© 2014 IEEE, with permission.)

to the value of the non-clocked input. Once X_3 settles to its final state, all metal lines are deactivated in the fourth phase. The voltages across the bitlines, sourcelines and wordlines during the different phases are shown in Fig. 7.3a. A 2-input XNOR (see Fig. 7.1c) can be similarly realized with ¬B written to X_1 and B to X_2. The rest of the procedures are similar to XOR. The XOR operation involves writing inputs in phase I followed by clocking in phase II. Phase III and IV involve releasing the clock. The total delay is t_w + t_c (see Fig. 7.3b).

During the entire operation, only two cells are written and two are clocked. If I_{sw} and I_{clk} are the average writing and clocking currents, the total energy is $2(I_{sw}t_w + I_{clk}t_c)V_{DD}$.

7.3.2 3-input XOR

In this section we have presented the new design for a 3-input XOR. The logic contains a total of 13 cells. The layout is shown in Fig. 7.4a. A, B and C are the inputs. Algorithm 5 summarizes the steps. For comparison, the traditional design is shown in Fig. 7.4b.

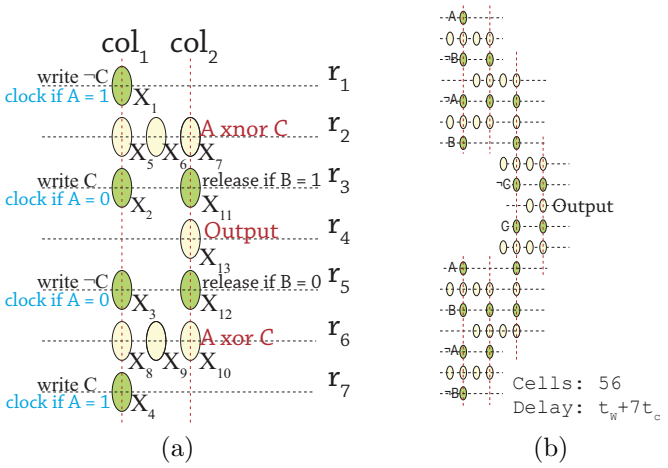


Figure 7.4: (a) New 3-input XOR; (b) Traditional design. (© 2014 IEEE, with permission.)

7.3.3 Novel Majority Design

In this section we have presented the design of a majority on similar lines. The layout is shown in Fig. 7.5a along with the traditional design in Fig. 7.5b. A, B and C are the inputs. The logic steps are summarized in Algorithm 6.

7.3.4 Analysis of the New Designs

The energy consumed by the new designs can be accounted to two sources:

(i) The metal lines that conduct writing and clocking currents; and

(ii) The CMOS peripherals that select the metal lines.

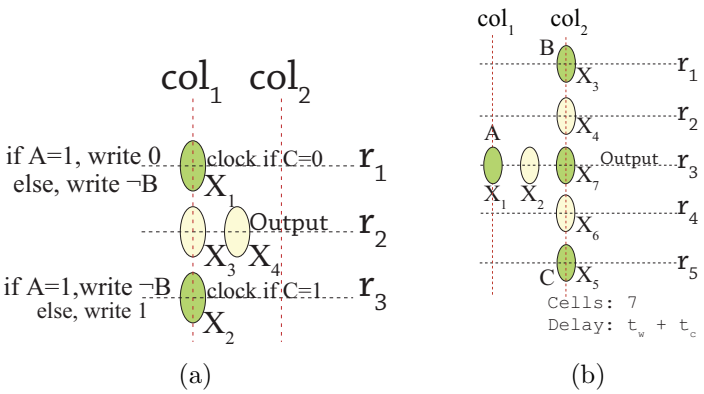


Figure 7.5: (a) New majority; (b) Traditional majority. (© 2014 IEEE, with permission.)

Input: A, B, C.
Output: $X_{13} = \text{A} \oplus \text{B} \oplus \text{C}$.
Phase I: Write to $X_1 = X_3 = \neg C$, $X_4 = X_2 = C$.
Phase II: Clock $X_5 \dots X_{10}$.
Phase III: Clock X_{11} & X_{12}
if $A = 1$ **then**
  Clock X_1 and X_4
else
  Clock X_2 and X_3.
end if
Phase IV: Clock X_{13}. Release clock for $X_5 \dots X_{10}$
Phase V:
if $A = 1$ **then**
  Release clock for X_1 and X_4
else
  Release clock for X_2 and X_3.
end if
if $B = 1$ **then**
  Release clock for X_{11}
else
  Release clock for X_{12}.
end if
Phase VI: Release the clock for X_{13}.
Phase VII: Deactivate all metal lines.

Algorithm 5: New 3-input XOR. (© 2014 IEEE, with permission.)

Table 7.1 presents a comparison of the cell count and the total delay between the new designs and the traditional ones. N_w and N_c refer to the number of writing and clocking

Input: A, B, C.
Output: Y_4 = A.B + B.C + A.C.
Phase I: Clock Y_3 and Y_4.
if $B = 1$ **then**
  Clock Y_2
  if $A = 1$ **then**
    Write $Y_1 = \neg A$
  else
    Write $Y_1 = \neg C$
  end if
else
  Clock Y_1
  if $A = 1$ **then**
    Write $Y_2 = \neg C$
  else
    Write $Y_2 = \neg A$
  end if
end if
Phase II: Release clock for Y_3 and Y_4.
Phase III: Deactivate all metal lines.

Algorithm 6: New Majority. (© 2014 IEEE, with permission.)

Table 7.1: Cell count and delay comparison. N_w and N_c are the number of writing and clocking cycles required in the proposed and traditional STT NML circuit designs in regular CMOS-MTJ architecture for XOR and majority. (© 2014 IEEE, with permission.)

Logic	Proposed Design: STT				Traditional Design: STT			
	Cell Count	N_w	N_c	Fig.	Cell Count	N_w	N_c	Fig.
2-input XOR	3	1	1	7.1b	16	1	3	7.1a
3-input XOR	13	1	2	7.4a	56	1	7	7.4b
Majority	4	0	1	7.5a	8	1	2	7.5b

cycles in the overall delay. Fig. 7.9a shows the reduction in cell count or area and delay of the new designs over their traditional ones. Table 7.3 presents the comparison of energy consumption, energy savings and EDP for three different logic circuits (2-input XOR, 3-input XOR and majority logic). In the table we have also included the energies required to operate the logic with the help of external fields. The energies with STT (E_{STT}) and Field (E_{field}) are calculated using the following equations.

$$E_{STT} = (n_w I_{sw} t_w + n_c I_{clk} t_c) \cdot V_{DD} \tag{7.2}$$

$$E_{field} = n I_f t_f \cdot V_{DD} \tag{7.3}$$

n_w and n_c refer to the total number of cells written and clocked with STT while n denotes the total number of rows that are written and clocked with field. The energy values reported in Table 7.3 include the energy consumed in the current carrying wires generating the fields. The percentage savings in energy achieved by the new designs for each of the three logic is shown in Fig. 7.9b. From Fig. 7.9a and Fig. 7.9b we see that the novel design style provides a greater improvement in terms of area, speed and energy for the XORs than the majority. This can be attributed to the binate nature of XOR. A binate logic function has a binate variable. And a binate variable is defined as one that is present in both complement and non-complement form within the function. Binate functions can fully utilize the potential of Shannon expansion and hence can gain more from this design style. The delay values (symbols are self explanatory) used in EDP calculations are obtained from Eq. 7.4 and Eq. 7.5.

$$t_{dSTT} = t_w N_w + t_c N_c \tag{7.4}$$

$$t_{dField} = (N_{wf} + N_{cf}) t_f \tag{7.5}$$

The values of t_w, t_c and t_f can be obtained from Table 7.2. N_{wf} and N_{cf} are the number of rows written and clocked with field.

Table 7.2: Current magnitudes and durations. These values are used to calculate the energy and EDP of the circuits. (© 2014 IEEE, with permission.)

Current	Duration	Purpose	Operation Type	I (μA)	t (ns)
I_{sw0}	t_w	Write 0	STT	-216	20×10^{-3}
I_{sw1}	t_w	Write 1	STT	278.9	20×10^{-3}
I_{cavg}	t_c	Clock	STT	170.5	3
I_f	t_f	Write & Clock	Field [87]	1.2×10^3	3

Table 7.3: Energy consumption and EDP values. The comparison is between various circuits with different designs and operation techniques. Please refer to Table 7.1 for figure references to proposed and traditional designs. (© 2014 IEEE, with permission.)

Logic	Proposed Design		Traditional Design	
	STT	Field	STT	Field
Energy consumption (in pJ).				
2-input XOR	1.03	14.4	4.62	32.4
3-input XOR	6.65	32.4	18.9	111
Majority	1.55	10.8	2.56	28.8
Full Adder	8.18	36	20.4	129.6
Energy Delay Product EDP (in Js).				
2-input XOR	$3.12e-21$	$8.64e-20$	$4.17e-20$	$3.89e-19$
3-input XOR	$4e-20$	$1.95e-19$	$3.97e-19$	$2.33e-18$
Majority	$4.65e-21$	$3.24e-20$	$1.54e-20$	$2.59e-19$
Full Adder	$4.31e-20$	$2.16e-19$	$4.3e-19$	$2.76e-18$

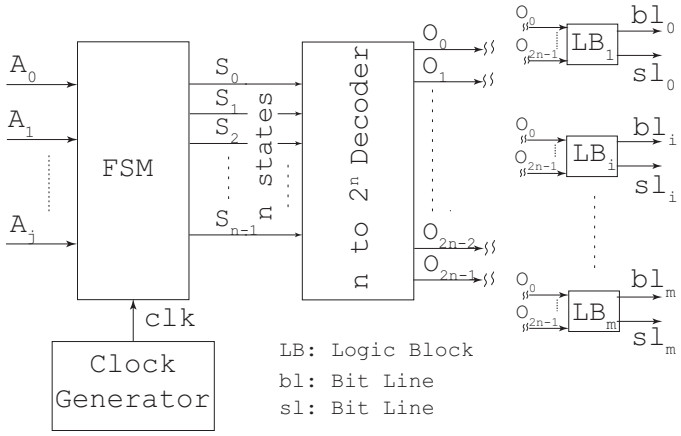


Figure 7.6: Block diagram of the CMOS peripherals. The CMOS is used to select bitlines for logic execution. Similar peripheral circuits are used for selecting sourcelines and wordlines. The peripheral circuits for the different metal lines differ only in the logic present in LBs to select the metal lines. (© 2014 IEEE, with permission.)

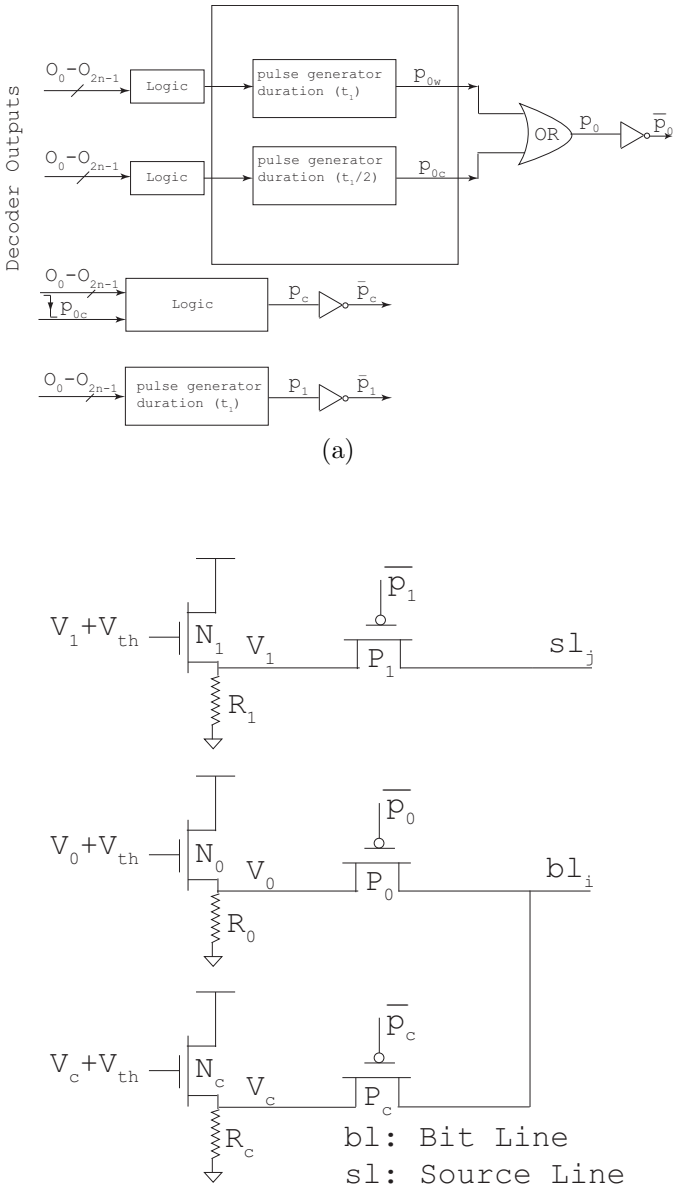
During the logic execution, in every clock cycle, a set of cells are clocked. The cells may all lie in a single row or in multiple rows. In either case bitlines, sourcelines and wordlines are selected with the help of CMOS peripherals, which also consume power. In this section we have provided an estimate of this power. The logic in the peripheral circuits are synthesized using 2-input AND/OR in 22nm PTM [94, 109, 110, 111]. The main components of the peripheral circuit are shown in Fig. 7.6. A_js are the inputs to the logic. The logic execution

is automatized with a FSM. The output from the decoder is used to control the voltage on the bitlines and sourcelines through logic blocks (LBs) that generate active high signals for writing, reading and clocking. Each logic block is made of a control signal generator (see Fig. 7.7a) and a voltage shifter (see Fig. 7.7b). The control signal generator takes the decoder outputs and generates control signals ($\neg p_1$, $\neg p_0$ and $\neg p_c$) of requisite durations. The signals are then used to sample the voltages to the metal lines.

In this chapter, we have considered the main sources of power consumption in the CMOS peripherals: the FSM, decoder, control signal generator, and the capacitive loads on the metal lines. The components excluded in the power calculation are the pulse generators and the voltage shifters that will be shared by different metal lines. Hence, their contribution to the overall power is much less significant. The power savings in the CMOS peripherals between the new and traditional designs has been shown in Fig. 7.8. A significant reduction in power in CMOS peripherals is observed, which accounts again to the reduced cell count in the new design. The improvement in area, speed and energy savings are shown in Fig. 7.9.

7.4 Conclusion

In this chapter we have discussed a Shannon expansion based logic partitioning scheme to boost the performance of datapath elements in the architecture. The key to the success of the new design scheme is the partitioning of logic responsibilities between the magnetic and the CMOS plane. In this chapter we have shown the new design rule for 2-input XOR, 3-input XOR and the majority. Benefits of the new design include drastic reduction in area, energy, delay, and reduction in power in the CMOS peripherals. In the next chapter we will discuss the second auxiliary role in STT-MRAM memories, where we have embraced the variations in memory to generate unique signatures for device authentication.



(a)

(b)

Figure 7.7: (a) The control signal generator; (b) The 3-level voltage shifter. The output of the control signal generator generates the control signals for the voltage shifter. (© 2014 IEEE, with permission.)

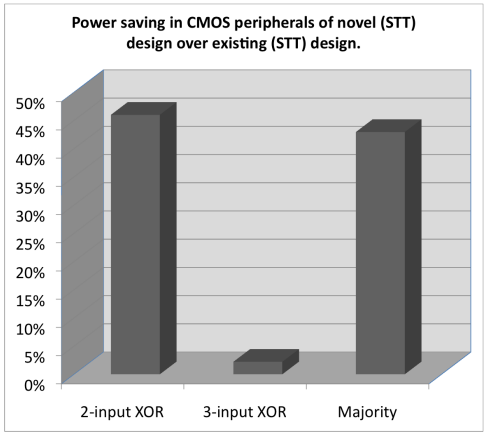
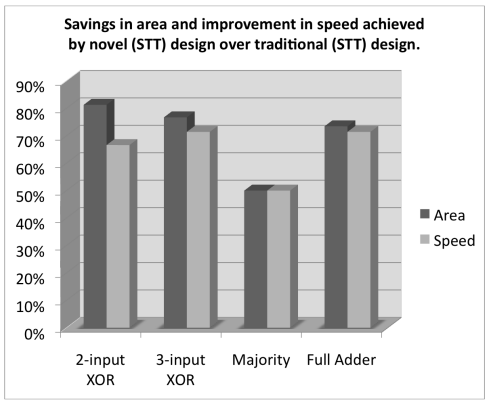


Figure 7.8: Power savings in CMOS peripherals. Comparison between the novel designs and the traditional designs. (© 2014 IEEE, with permission.)



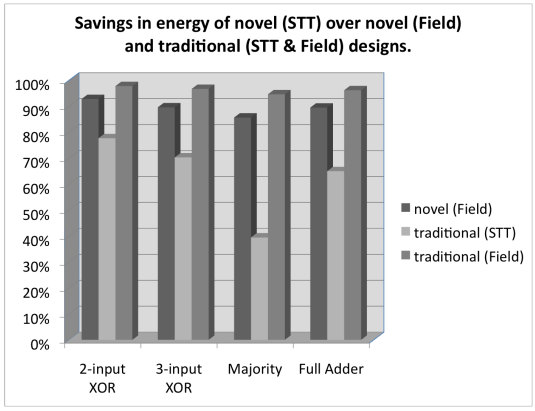


Figure 7.9: Performance improvement with logic partitioning. (a) Improvement in area and speed in the magnetic plane achieved by the novel designs over the traditional STT designs; (b) Savings in energy in the magnetic plane achieved by the novel designs over each of their novel (field) and traditional (STT and field) counterparts. (© 2014 IEEE, with permission.)

CHAPTER 8

AUTHENTICATION USING STT-MRAM

8.1 Motivation

Security is one of the main concerns as more and more heterogenous devices are connected to each other in a network. Device authentication has therefore become increasingly important to prevent malicious attacks on the network. Using intrinsic variations within device to generate unique signatures without storing them anywhere in the device is a way to authenticate the device. Variations being random across devices also prevents an adversary to predict the signature of a device. Here we have discussed a novel way of using the intrinsic variations within the STT-MRAM cells to generate digital signatures.

8.2 Physically Unclonable Functions (PUFs)

A PUF can be best defined as "an expression of an *inherent* and *unclonable instance-specific* feature of a physical object" [112]. This implies: (i) a PUF is inherently created at the time of creation of an instance of an object; (ii) there is no user control over its creation; (iii) it is unique and specific to every instance; and (iv) creating two PUF instances puf_{i_i} and puf_{i_2}, $i_1 \neq i_2$, that produce the same response is not feasible.

Two terms are closely associated with PUF usage [112]:

(i) challenge: this is an input $\text{x}_k \in \mathcal{X}_\mathcal{P}$ to the PUF;

(ii) response: this is the output y_i of puf_i in response to the challenge x_k.

[0]This chapter was published in IEEE Conference on Nanotechnology, 2014, " A Novel Geometry Based MRAM PUF", Jayita Das, Kevin Scott, Drew Burgett, Srinath Rajaram, and Sanjukta Bhanja.

The process of reading out from a PUF is called "evaluating" the PUF. There are two statistical parameters which determine the usability of a PUF class $\mathcal{P}$, where $\text{puf}_i \in \mathcal{P}$.

(i) Intra-distance $\mathcal{D}_{intra}$: is the hamming distance or the fractional hamming distance between two random evaluations $\text{y}_i^{j_1}$ and $y_i^{j_2}$, $\text{j}_1 \neq \text{j}_2$, of a single PUF instance puf_i for the same challenge $\text{x}_k \in \mathcal{X}_\mathcal{P}$.

(ii) Inter-distance $\mathcal{D}_{inter}$: is the hamming distance or the fractional hamming distance between evaluations $y_{i_1}^j$ and $y_{i_2}^j$ of two different PUF instances puf_{i_1} and puf_{i_2}, $\text{i}_1 \neq \text{i}_2$, for the same challenge $\text{x}_k \in \mathcal{X}_\mathcal{P}$ [112].

A PUF class $\mathcal{P}$ should also display certain basic properties. Informal quantifiers like easy, hard, high and low are typically used to define these properties.

(i) Constructibility: Constructing a random PUF instance puf_i should be easy.

(ii) Evaluability: Evaluating the response of any PUF instance puf_i to a random challenge $\text{x}_k \in \mathcal{X}_\mathcal{P}$ should be easy.

(iii) Reproducibility: When evaluated multiple times, a PUF puf_i should generate the same response y_i to the same challenge with a high probability i.e. for high reproducibility a PUF instance should have a low $\mathcal{D}_{intra}$.

(iv) Uniqueness: Response of two different PUF instances to the same challenge, $\text{y}_{i_1}^j$ and $\text{y}_{i_2}^j$ should be highly dissimilar, i.e. a PUF class should have a high $\mathcal{D}_{inter}$. Uniqueness ensures that it is hard for an adversary to predict the response y_{i_2} of puf_{i_2} from his/her prior knowledge of response y_{i_1} of puf_{i_1} to the same challenge x_k, $\text{i}_1 \neq \text{i}_2$.

8.2.1 Memory Based PUFs

The most popular memory based PUF is the SRAM PUF. An SRAM cell is composed of a cross-coupled inverter latch. For desired operation, designers ensure the best possible

symmetry between the inverter pairs. However, variations in process technology result in a device mismatch. This mismatch is random but specific to every SRAM cell [113]. It generates a preferred power-up state in every cell that is used to build the SRAM PUF. The other common memory based PUF is the latch PUF where the mismatch between two cross-coupled NOR gates is used to generate the PUF response [114].

Nanoscale PUFs based on memristive crossbars have been proposed that utilize the uncontrollable variations in the thickness, area, and concentration of the insulating materials used in memristors and the associated randomness in write voltages and pulse durations [115, 116]. The preliminary results on these PUFs are carried out through modeling and simulation and suggests good uniformity and uniqueness [117, 116]. Nanoscale memory PUFs using resistive variations of STT-MRAM cells have also been proposed [118]. However, the PUF responses are stored in the non-volatile memory. The studies are also simulation based and show good uniqueness and randomness.

8.3 Theory of MRAM PUF

The MTJs in STT-MRAM are patterned with a shape anisotropy to give them two stable ground states at room temperature (see Fig. 8.1a) separated by an energy barrier E_b, which accounts for the thermal stability Δ in the cells (Eq. 8.1) [16].

$$\Delta = \frac{H_k M_s V}{2 k_B T} \tag{8.1}$$

Let us now have a deeper understanding of this energy landscape to see how it can be used to generate unique signatures. Fig. 8.1 shows MTJ free layers and their corresponding energy landscape. At this point we will assume that all the remaining layers in the MTJ are of perfect geometry. In fact, assuming variations in their geometries would further enhance the unpredictability in the PUF response. In Fig. 8.1a, the free layer has a perfect geometry. The ground states are positioned symmetrically across the energy barrier. Consider the

position A, which is also the hard axis of the free layer. If the magnetization is released from A, it will have an equal probability to settle down into one of the two ground states. The probability of 1 and 0 would be equally likely in this case.

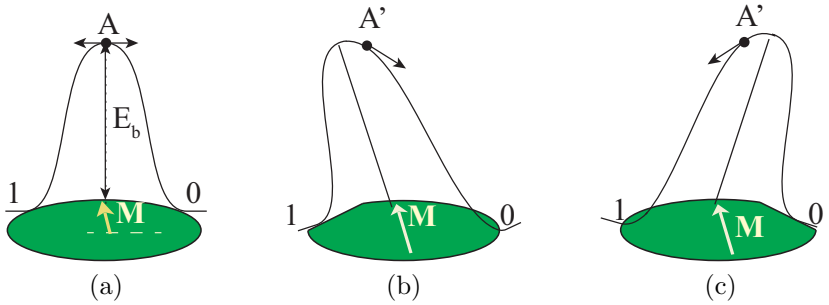


Figure 8.1: Energy landscape for different MTJ geometries. (a) Perfect geometry. (b) and (c) Random variations in cell geometry. For (b) and (c) the magnetization at location A' develops a preference for one of the ground states. (© 2014 IEEE, with permission.)

Now consider the case of process variations that affect the geometry of the free layer. This in turn would affect the energy profile of the cell. The outcome is a tilt in the easy axis of the cell [67], which makes A' more likely to settle for one of the ground states than the other. This variation is random from cell to cell and is not predictable. We have used this variation in cell geometry to generate unique digital signatures from MRAM cells [119].

8.4 MRAM PUF Operating Principle

In the previous section we have seen that the MTJs develop a preferential ground state as a result of random process variations affecting the cell geometry. In this dissertation we have used this information about preferential ground states in cells to generate unique digital signature out of MRAM PUF. To extract this information we need to first take every cell to its hard axis. To do this we have borrowed the concept of clock that we have already discussed in Chapter 2 and Chapter 4. A clocked MTJ when released would settle for its preferential ground state. Reading a set of these cells can give us a unique signature that we can use for authentication. The dynamics of the free layer upon release from clocked state will be governed by Eq. 8.2.

$$\frac{d\mathbf{M}}{dt} = -\gamma \mathbf{M} \times \mathbf{H_{eff}} + \alpha \mathbf{M} \times \frac{d\mathbf{M}}{dt} \tag{8.2}$$

$\mathbf{H_{eff}}$ is the effective magnetization field on the layer generated from a combination of anisotropy ($\mathbf{NM}$), external fields ($\mathbf{H_{Zeeman}}$) and thermal effects ($\mathbf{H_{therm}}$).

$$\mathbf{H_{eff}} = \mathbf{NM} + \mathbf{H_{Zeeman}} + \mathbf{H_{therm}} \tag{8.3}$$

In Eq. 8.3, $\mathbf{N}$ is the demagnetization tensor, which takes into account the shape anisotropy of the cell [120]. For an ellipsoid with axes (a>b>c), $\mathbf{N}$ is given by a diagonal matrix (Eq. 8.4), where each term is defined by Eq. 8.5. $\mathbf{H_{therm}}$ is given by Eq. 8.6 [121]. The symbols in the equations are explained in Table 2.3.

$$\mathbf{N} = \begin{bmatrix} \mathbf{N_a} & 0 & 0 \\ 0 & \mathbf{N_b} & 0 \\ 0 & 0 & \mathbf{N_c} \end{bmatrix} \tag{8.4}$$

$$\mathbf{N_i} = \frac{1}{2} abc \int_0^\infty \left[(i^2 + \eta) \sqrt{(a^2 + \eta)(b^2 + \eta)(c^2 + \eta)} \right]^{-1} d\eta \tag{8.5}$$

$$\mathbf{H_{therm}} = \frac{1}{\sqrt{V \Delta t}} \sqrt{\frac{2 k_B T \alpha}{\mu_0 \gamma M_s}} \mathbf{g(t)} \tag{8.6}$$

and $\mathbf{g(t)}$ is a Gaussian distributed random vector.

8.5 Sources of Bias and their Elimination

There are two possible sources of coupling that can produce a biased response. One is the dipolar coupling from the fixed layer and the other is the coupling from neighboring MTJs. Both these biases contribute to $\mathbf{H_{Zeeman}}$. For unbiased responses $\mathbf{H_{Zeeman}}$ should be $\ll \mathbf{NM} + \mathbf{H_{therm}}$ and the preferential ground state of the cells should be determined

by the variations in the shape anisotropy **NM** and the random thermal vector $\mathbf{H_{therm}}$. Our objective is therefore to reduce $\mathbf{H_{Zeeman}}$ and eliminate the biases. Dipolar coupling from fixed layer can be reduced with proper choice of the thicknesses of the fixed and the pinning layer [122]. Reducing the dipolar coupling from the fixed layer would also allow the dynamics of the free layer to be replicated by a single layer nanomagnet. Henceforward, for all experimental and simulation results that we will be discussing in this chapter, we would be referring to single layer cells unless we explicitly mention.

Inter-cell coupling can be reduced by placing the MTJs sufficiently far apart as they are usually done in memory. Fig. 8.2 shows simulation results using OOMMF, for two different spacing between cells in a 2×2 array. When the cell spacing is 20nm, the cells clearly display a ferromagnetic and antiferromagnetic coupling. When the spacing is increased to 250nm no effective coupling is visible between the cells. The cell sizes were $60 \times 90\text{nm}^2$ to match our fabrication efforts [119].

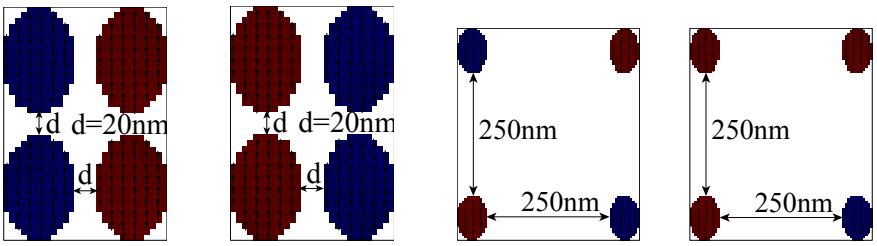


Figure 8.2: Coupling with cell separation. (a) and (b) Effective dipolar coupling between the $90\times60\text{nm}^2$ cells spaced 20nm apart. (c) and (d) No effective coupling between cells $90\times60\text{nm}^2$ spaced 250nm apart. (Images not drawn to scale). (© 2014 IEEE, with permission.)

Fig. 8.3a demonstrates the desired forces acting on the free layer at the point of its release from the hard axis. Fig. 8.3b shows that with increase in the variations of the cells, the error in the responses get reduced. The error refers to the cell settling for its non-preferred ground state when released from the clocked state. The results were obtained from simulations carried out in OOMMF. The results indicate that with increase in variations or greater tilt angles the errors from thermal noise get masked. Therefore to generate reproducible results

it would be beneficial to select cells with higher deformations. This selection can be based on multiple initial runs prior to the deployment of the sample in field.

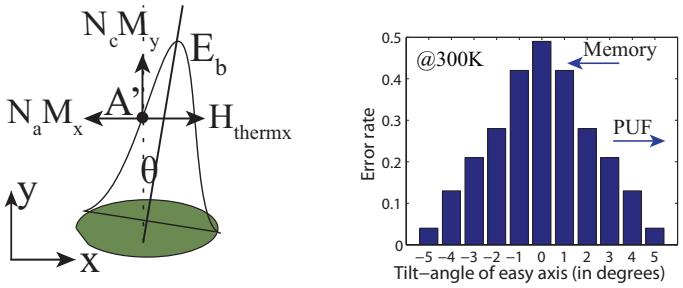


Figure 8.3: PUF operation and error rate. (a) Energy profile of a PUF cell that has a deformation on left. The forces acting on the cell at the instant when it is released from its hard axis. The preferred state for the cell is determined by ($\mathbf{N_aM_x}$ - $\mathbf{H_{thermx}}$). (b) Error rate @300K in PUF cells ($90 \times 60 \times 5\text{nm}^3$) against tilt angle in easy axis. The arrows show the orthogonal requirements of variations between memory and PUF. (© 2014 IEEE, with permission.)

8.6 Destabilization Technique in STT-MRAM PUF

We have already seen in the last section that the MTJs to be used fpr PUF should not have any coupling from the fixed to the free layers. In Section 4.3 we have studied the coupling requirements from the fixed layer in order to implement the STT clocking, where the cells need to have a tilted polarized fixed layer. The requirements of PUF and clock are therefore not supportive of one another. Moreover for generating a digital signature, we would select a row of cells. STT clocking of a row of n cells would require n$\times$ $I_{stt\_clk}R_{avg}$ amount of power, where R_{avg} is the resistance of a cell. For large n, this would outnumber any benefit from low power STT clocking that we have for small number of cells clocked together in logic. However, for field based clocking, the clocking power for a row of cells is given by $I_{clk}R_{avg}$ and is independent of the number of cells in the row.

In this section we have discussed how to clock a STT-MRAM cell using magnetic fields. Fig. 8.4 shows a cross-section of a STT-MRAM cell. The bitline is connected to the free layer of the MTJ while the sourceline is connected to the source of the access transistor. The

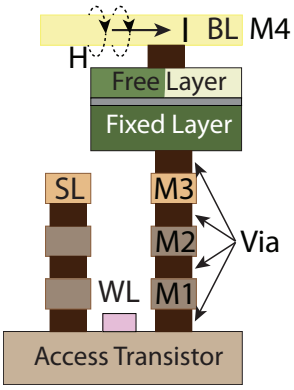


Figure 8.4: Cross-section of a STT-MRAM cell.

wordline is connected to the gate of the access transistor. The bitline runs parallel to the easy axis of the MTJ. Therefore, with a required current I_{clk} flowing only through the bitline of the MTJ we can generate a magnetic field directed along the hard axis of the MTJ. In order to ensure that no current flows through the MTJ, the wordline of the MTJ needs to be grounded in order to keep the access transistor turned off.

8.7 Results and Analysis

8.7.1 PUF Evaluation

8.7.1.1 Entropy

To determine the randomness in the PUF response we have calculated the entropy density function $\rho(Y^n) = \frac{H(Y^n)}{n} = -\frac{1}{n}\sum_{i=1}^{n}((p_i)log_2(p_i) + (1-p_i)log_2(1-p_i))$ [112] from evaluations of our fabricated array. A $\rho(Y^n)$ of 0.9997 (see Table. 8.1) was obtained from the array, which indicated a very high randomness in the PUF response.

8.7.1.2 Constructibility

Constructibility is the ease to build the PUF. This PUF is easily constructible since it does not require any additional processing steps over the memory. Geometric variations are something all MTJs are subjected to and this PUF utilizes these variations to generate its

responses. The only step that is beyond the normal memory operation is the destabilization procedure, which again can be easily carried out using the metal lines in the array. Only minimal hardware and current drivers beyond conventional memory will therefore be required to supply the destabilizing current.

8.7.1.3 Evaluability

The evaluation of the PUF is also very straight forward. Once an authentication request comes from the processor, the following two steps are to be carried out over the PUF cells: (i) destabilization; followed by (ii) release and relaxation. The PUF response can be read out using the standard memory read techniques [123].

8.7.1.4 Reproducibility

The measure of reproducibility in PUF is the intra-distance $\mathcal{D}_{intra}$. We repeated the PUF evaluation process using the stochastic LLG simulations over SEM images of our fabricated array to evaluate $\mathcal{D}_{intra}$ [119]. A total of 20 cells were selected and the simulations were repeated 40 times over the 20 cells. With this process an average $\mathcal{D}_{intra}$ of 0.0225 was obtained. This low $\mathcal{D}_{intra}$ indicates a good reproducibility in the responses of the PUF.

8.7.1.5 Uniqueness

The measure of uniqueness for the PUF is the inter-distance, $\mathcal{D}_{inter}$. Once again we used stochastic LLG simulations over SEM images of three sets of 4×5 section of our fabricated arrays. A $\mathcal{D}_{inter}$ of 0.47 was obtained indicating a high uniqueness.

8.7.1.6 Area

The PUFs have a significantly small footprint as well compared to other silicon PUFs. Table 8.1 compares the area between different 64-bit PUFs.

Table 8.1: PUF comparison. MRAM PUF against different silicon PUFs [124] and nano PUFs [116, 118]. The area is for 64-bit length of response.

PUF Types	$\mathcal{D}_{intra}$	$\mathcal{D}_{inter}$	$\rho(Y^n) \leq$	area (μm^2)
SRAM	0.078	0.49	0.94	51.99
Latch	0.26	0.3	0.71	531.25
D flip-flop	0.19	0.39	0.81	765.63
Arbiter	0.07	0.46	0.5-0.9	690.56
Ring Oscillator	0.099	0.46	0.86	7774.2
Memristor *	–	$\simeq 0.5$	–	–
STT-PUF *	$\sim$ 10e-6	$\simeq 0.5$	0.985	6.79
MRAM	0.0225	0.47	0.99	6.74

* These PUFs were not fabricated. Their behavior is estimated only through simulated models.

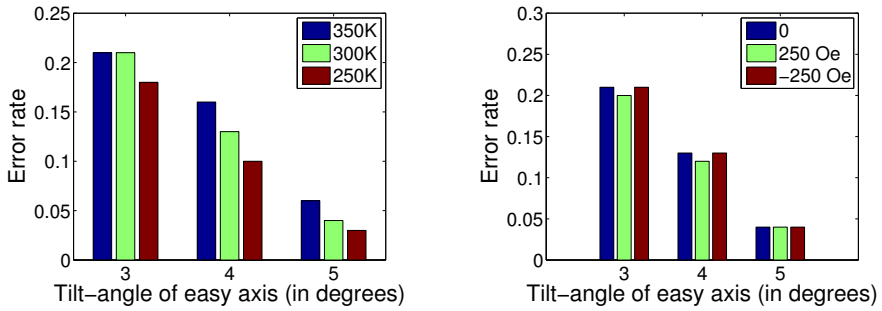


Figure 8.5: Error rate with temperature and variation in fixed layer thickness. (a) Error rate in PUF cells at different temperatures; (b) Error rate in PUF cells with thickness variation in fixed layer. The thickness variation was modeled with the help of resultant coupling field on the free layer. In both cases a cell size of $90 \times 60 \times 5nm^3$ was simulated.

8.7.2 Robustness Analysis

For the desired reproducibility in the MRAM PUF response, cells with tilt angles $-3^\circ \geq \theta \geq 3^\circ$ are preferable and need to be selected for PUF (see Fig. 8.3b). Once again we have used stochastic LLG simulations in OOMMF over a cell with tilt angle between $-3^\circ \geq \theta \geq 3^\circ$ to analyze the robustness of the cell to thermally induced errors. We have also explored the geometric parameters for the cells that can enhance the robustness. Each reported error rate $\mathcal{E}$ was obtained by calculating the normalized hamming distance over 100 simulations for each $\theta_i \geq 3^\circ$. For a n-bit PUF, the error rate $\mathcal{E}$ is related to $\mathcal{D}_{intra}$ as $\mathcal{D}_{intra} = \frac{1}{n}\sum_{i=1}^{n} \mathcal{E}_i$.

8.7.2.1 Robustness with Temperature

As we have mentioned in Section 8.3, the thermal vector $\mathbf{H_{therm}}$ can influence the ground state if it is greater than or equal to **NM**. However, we have simulated the response of the PUF cell for only $-3^\circ \geq \theta \geq 3^\circ$ where the value of **NM** is reasonably large. Fig. 8.5a shows the error rate in the PUF cells with temperature. With an increase of 50K over room temperature, a maximum increase in error rate of only 0.03 is observed at θ=4°. On the other hand, the error rate decreases with decreasing temperature. Therefore, we can safely conclude that the PUF is robust across wide ranges of temperature.

8.7.2.2 Robustness with Variations in Fixed Layer

Fig. 8.5b shows the error rate with variation in the fixed layer thickness. This causes a non-zero coupling on the free layer of the MTJs. Here we have considered a conservative coupling field of ±250Oe on the free layer from the fixed layer. From Fig. 8.5b we see that the error rate changes by a negligible fraction with coupling from the fixed layer indicating that the PUF is robust to the variations in the thickness of the fixed layer.

8.7.2.3 Robustness Enhancement with Geometry

In this section we have explored the geometric parameters that can help to improve the PUF robustness. Our goal is to increase the ($\mathbf{N_a M_x}$ - $\mathbf{H_{thermx}}$) margin for the cells. This implies either (i) increasing $\mathbf{N_a}$, which is a function of shape anisotropy (a/b) of the cell; or (ii) decreasing $\sigma_{\mathbf{H_{therm}}}$, which is a function of the volume V of the cell (Eq. 8.6).

(i) Increasing the volume @ constant aspect ratio: Increasing the volume decreases the $\sigma_{\mathbf{H_{therm}}}$ term and increases the ($\mathbf{N_a M_x}$ - $\mathbf{H_{thermx}}$) margin. Fig. 8.6a shows the error rate with different thicknesses at constant area. A sharp fall in error rate by 0.24 is seen at $\theta = 5^\circ$, when the thickness is increased from 2nm to 5nm. A considerable drop of 0.11 at θ=5° is also observed for thickness increase from 2nm to 3nm. Fig. 8.6b

shows the error rate for different cell areas at constant thickness. A maximum error reduction of 0.1 is seen at θ=3°, when the cell area is increased from $90 \times 60\text{nm}^2$ to $120 \times 80\text{nm}^2$.

(ii) Decreasing the aspect ratio @ constant volume: This increases $\mathbf{N_a}$ while keeping $\sigma_{\mathbf{H_{therm}}}$ constant. However, as seen from Fig. 8.6c, this method is not very effective in enhancing the PUF robustness.

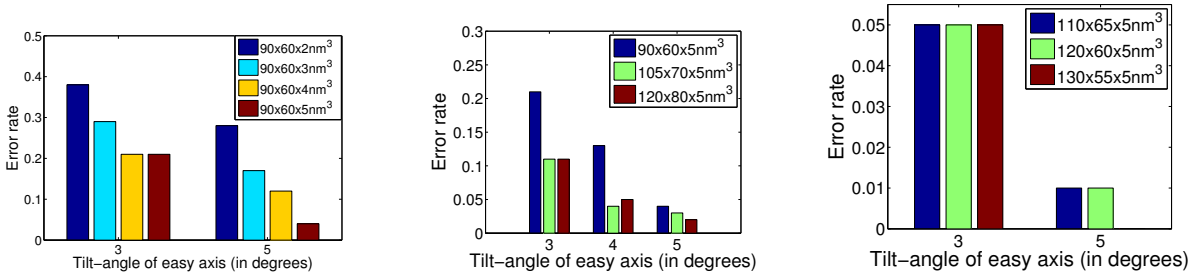


Figure 8.6: Error rate with different geometric variations. (a) Error rate in PUF cells at 300K for different thicknesses of the free layer; (b) Error rate in PUF cells at 300K for different cell areas with same 3 : 2 aspect ratio; (c) Error rate in PUF cells at 300K for different aspect ratios with same cell area.

8.8 Conclusion

In this chapter we have described the second auxiliary role for STT-MRAM. We have discussed how intrinsic geometric variations in the cells can be used to generate unique digital signatures that can be used for authentication. We have also discussed the PUF evaluation procedure that involves temporarily destabilizing the cells and then releasing them. Methods to reduce any biases in the responses have also been discussed. The PUF has exhibited a high $\mathcal{D}_{inter}$ and a low $\mathcal{D}_{intra}$ indicating both high uniqueness and reproducibility. Finally, we have discussed various techniques in which we can improve the reproducibility of the STT-MRAM PUF responses.

CHAPTER 9

CONCLUSION

9.1 Synopsis

The unique properties of STT-MRAM together with its growing success and the global investments have increased its potential to become a universal memory. In this dissertation we have studied two ways in which we have used the intrinsic properties of the technology into roles beyond traditional storage that can benefit the overall computing system. First, we have designed a logic-in-memory architecture where these cells can switch between logic and memory modes of operation with the help of a control signal. Second, we have used the random variations within the STT-MRAM cells to generate digital signatures that can be used for authentication purposes.

The role of the architecture is to compute only when clocked and to store when unpowered. In the architecture design the memory cells are brought within interacting distance for computation. We have discussed the technology constraints faced for bringing the cells closer to one another and how we have resolved the constraint by careful choice of CMOS technology node and integration of access transistors. Depending on the functionality the architecture cells have been labeled as inputs, outputs and logic. Layouts of elemental logic blocks and interconnects in the architecture have also been discussed. To clock selected group of architecture cells, a low power spin transfer torque clock has been proposed and analyzed. It is based on a stationary equilibrium state of the cells induced by spin transfer torque and coupling from underneath fixed layer. We derived the clocking current from the fundamental constraint of magnetization and the LLG equation governing the magnetody-

namics of the free layer. A variability tolerant differential read circuit for the architecture has been proposed. The read circuit works in two phases, the precharge phase followed by the sense phase. It compares the output state against its complement. To reduce variation effects in the read circuit we have introduced redundancy by reading a pair of outputs against a pair of complements. The read circuit is low power and is non-destructive with the cell states retained after read.

Simulation tools are available for standalone CMOS and magnetic technology. Moreover, the available magnetic simulator OOMMF facilitates only micromagnetic simulation that is good for verifying physical properties but is not fast enough to verify larger circuits. A macromagnetic model that can be integrated with CMOS simulator can help in fast simulation of the architecture. The Verilog-A model described in this dissertation is the solution to this. To further address the low energy needs, we have discussed some of the possible energy reduction techniques for the architecture. We have also discussed a layout constraint and a clock distribution constraint that affects the layout flexibility and improves the performance of the architecture. Solutions to the problems are provided in terms of selected irregularity within layout and a 4-phase clock. Finally we have discussed a logic partitioning scheme aimed at distributing the logic responsibilities between the magnetic and the CMOS planes in the architecture. The distribution relies on Shannon expansion of logic and is aimed at improving the performance of data path elements in the architecture.

Variations from process technologies are unavoidable and mostly a concern for designers. In this dissertation we have followed a different route and used the variations to generate signatures. We have used the intrinsic geometric variations in STT-MRAM cells that alters the symmetry in their energy landscape and generates a preferred ground state in the cells. This preferred state is random and unclonable. We have used this hidden information in the cells for developing STT-MRAM PUF. We have shown that this information can be extracted by first destabilizing the cells and then releasing them so that they settle down to

their preferred ground state. Performing this operation over a row of memory cells can give a n-bit binary string, which can then be used as signature for authentication.

9.2 Future Work

In future we would like to explore at a systemic level the computation and authentication operations with STT-MRAM. One of our objectives would be to identify the best possible memory locations for authentication and the best levels of memory where the operation can be carried out. As of computation one of our goals is to figure out the optimum computation that can be performed in memory to alleviate the Von Neumann bottleneck. Reconfigurability within the computing architecture is our other goal. Finally with development in CMOS technology nodes, our goal would be to further optimize the integration of access transistor and increase their density for better cell selectivity in the architecture.

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Appendix A (Continued)

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Title: Low power CMOS-magnetic nano-logic with increased bit controllability

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Title: Addressing the layout constraint problem when cascading logic gates in nanomagnetic logic

Conference Proceedings: Nanotechnology (IEEE-NANO), 2012 12th IEEE Conference on

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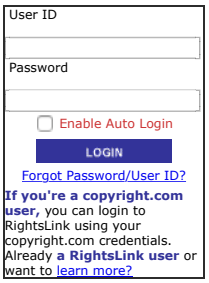

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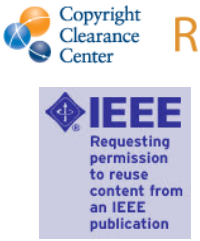
Appendix A (Continued)



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